

**OBJECTIVE**

To secure a technically challenging internship position.

**EDUCATION**

UNIVERSITY OF MASSACHUSETTS, AMHERST

**MASTERS IN ELECTRICAL ENGINEERING**

**(Feb 2008)**

**GPA 3.5/4**

**PHD IN ELECTRICAL ENGINEERING**

**(Expected Graduation: Feb 2010)**

UNIVERSITY OF MADRAS, CHENNAI, INDIA

**BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION, WITH DISTINCTION**

**GPA 3.8/4**

**(2000 - 2004)**

**SKILL SET**

Programming Languages: Fortran 90, Perl, C, C++, Matlab, and Lex & Yacc

EDA tools: Cadence tools (VirtuosoXL, VerilogXL, IRSIM, HSPICE, Spectre, Awaves),

Synopsys (Primitime, Design Compiler), PSPICE

Hardware Languages: Verilog, VHDL

Operating Systems: Aix, Unix, Linux

Application Packages: DAMOCLES, LaTeX

**RESEARCH**

*Current:* Working on **Quantum Transport** in thin slabs and emerging devices like **nanowires**.

*M.S. Thesis Title:* **Interband and gate tunneling in "Unconventional" MOSFETs.**

Estimation of **Zener** tunneling currents in sub-80 nm bulk and **SOI** MOSFET devices using **Monte-Carlo** simulations

Estimation of gate leakage currents in **high- $\kappa$**  dielectric stack of insulators and ultra-thin oxides

*Thesis Advisor:* Massimo V Fischetti

**PROJECTS UNDERTAKEN**

**Calculation of band structures of FCC semiconductors (Spring 2006)**

Employed local empirical pseudopotentials to calculate the bandstructure of the semiconductors like Si, Ge, InAs and InGaAs among others along a particular path in the Brillouin zone. The effective mass in X, L and G valleys was evaluated for various semiconductors.

**Monte-Carlo simulation of electron scattering in MOSFET channel (Spring 2005)**

Full Monte-Carlo simulation of electron scattering in an n-type doped Si MOSFET was performed in one dimension. The simulation included acoustic and optical phonon scattering and impurity scattering models.

**Interconnect design for secure MP-SOC (Spring 2005)**

Worked in a team of four to design and implement a MP-SOC using HSPICE and Verilog HDL (at 70 and 45 nm technologies) that were secure against a host of attack mechanisms. The design worked optimally at a clock frequency of 400 MHz.

**Design of memory BIST controller (Fall 2005)**

Worked in a team of two to design and implement an FSM to run a memory BIST controller that applied March C tests on a 256-bit SRAM. The design was implemented using Verilog-XL.

**Design of multi-sampling latches (Fall 2005)**

Worked in a team of three to design and implement a novel RAZOR latch that was robust and fault tolerant by incorporating temporal sampling technique. The error probability was found to be less than 5 % in the wake of process variations. The design was implemented using HSPICE, Verilog and Perl.

**Fault simulation of ISCAS benchmark circuits (Fall 2005)**

ISCAS benchmark circuits were read using a lexical analyzer and a parser (Lex and Yacc) and converted to nets. Sequential fault simulation was then performed on these nets.

### **Low power Kalman filter for signal estimation in cryptography (Fall 2004)**

Worked in a team of two to design a novel LRNS number system based low power Kalman filter to estimate signals in a noisy environment. A real number convolution code was used to encode and decode the signals.

### **RECENT PUBLICATIONS**

- S. Narayanan, C. Sachs and M. Fischetti, “*Study of performance and leakage currents in nanometer-scale bulk, SOI and double-gate MOSFETs*”, Journal of Computational Electronics, Vol. 7, 24(2008).
- M. Fischetti, S. Narayanan, et al., “*Theoretical study of some physical aspects in nMOSFETs at 10nm gate-length*”, IEEE Trans. Electron Devices, Vol. 54, No. 9, 2116(2007).
- M. Fischetti, S. Narayanan, et al., “*Electron transport in engineered substrates: strain, orientation, and channel/insulator material effects*”, Journal of Electro-Chemical Society 2006.

### **PRESENTATIONS AND TALKS**

- “*Leakage Concerns in Sub-80 nm Double-gate and Bulk MOSFETs*”, S. Narayanan, C. Sachs and M. Fischetti, TECHCON 2007, Austin, Texas, Sep 10-13, 2007.
- “*Electronic transport in "unconventional" SOI MOS systems: Thin-body and high- $\kappa$  effects in Si, Ge, and III-V layers*”, INVITED, M. Fischetti, S. Narayanan, et al., Electrochemical Society International Conference on: SOI Device Technology, Chicago, Illinois, May 6-11, 2007.
- “*Electron Transport in Engineered Substrates: Strain, Orientation, and Channel/Insulator Material Effects*”, INVITED, M. Fischetti, S. Narayanan, et al., Electrochemical Society International Conference on: SiGe: Materials, Processing, and Devices, Cancún, Mexico, October 29-November 3, 2006.
- “*Electron Mobility in Engineered Substrates: Strain, Orientation, and Channel/Insulator Material Effects*”, INVITED, M. Fischetti, S. Narayanan, et al., European Material Research Society Meeting, Nice, France, May 29-June 2, 2006.

### **COURSES TAKEN**

- *Solid State Devices*: Fundamentals of Solid State Electronics I and II, Semiconductor Devices, Numerical Modeling of Semiconductor Devices, Intermediate Quantum Mechanics II.
- *Digital Design*: Introduction to VLSI design principles, Advanced VLSI Design, Testing and Diagnosis of VLSI Systems, Physical Design and Automation of VLSI circuits, Microelectronic Fabrication.

### **WORK EXPERIENCE**

- **Software Engineer**, [Motorola India Electronics Limited](#), Bangalore, India (2004)  
Worked as a Software Engineer in Motorola India Electronics Limited to develop software for Motorola mobile handsets.
- **Electronics Engineering Intern**, Broadcasting Corporation of India Doordarshan Kendra, Chennai, India (Dec 2002)  
Worked as an intern and learnt about the practical operation of an uplink station. Learnt about digital and analog modulation schemes and satellite transponders.
- **Research Trainee, Waran Research Foundation (WARFT)** (Sep 2002 - Dec 2004)  
Was a part of ‘Charaka’ group that aimed at merging electronics, signal processing and computational neuroscience to develop supercomputing systems. Was involved with modeling the information processing of the hippocampus in the brain as a Kalman Filter.

### **HONORS AND ACHIEVEMENTS**

- Ranked 2422 out of 150,000 students in All India IIT-JEE 2000 Examination.
- Published three peer-reviewed conference papers on VLSI applications in neuroscience.
- Awarded merit certificate by National Scholarship Scheme for being in top 0.1% in India in Board Examination conducted by CBSE in 2000.