

Programmable Current Source Dedicated to Implantable Microstimulators

J-C. Voghell, M. Sawan, M. Roy and S. Bourret

Department of Electrical and Computer Engineering, École Polytechnique de Montréal,
P.O.Box 6079, Station « Centre-ville », Montréal, Québec, Canada, H3C 3A7
Fax: (514) 340-4147. E-mail: voghell@vlsi.polymtl.ca

Research area — Design and application of integrated circuits and systems

Abstract — In this paper, a survey of programmable current-source architectures based on miniaturized digital-to-analog converters (DAC) is elaborated to propose a new design dedicated for a visual microstimulator. The needed current-source constitutes the electronic interface to tissues. Few samples of this current-source will be integrated in the implantable device which is powered and controlled using an electromagnetic coupling technique. The main objective is to select a design that meet as close as possible criteria related to the implant such as reliability, flexibility, energy efficiency and integration area. Consequently, an adequate current-source is proposed which is a 5-bit thermometer-code-based DAC architecture. The resulting circuit is simulated using the 0.35 μ m CMOS technology from PMC-Sierra available through Canadian Microelectronics Corporation (CMC).

I. INTRODUCTION

Significant advances have been made in demonstrating the feasibility of using electrical stimulation to restore lost motor, visceral or sensory functions. In order to help blind individual to recover a functional vision by intracortical stimulation through an array of microelectrodes, a permanent implant controlled by electromagnetic signals is needed [1], [2], [3]. Electrical stimulation of the visual cortex produces localized visual perceptions called phosphenes. The overall system is a fully integrated implantable system composed of 25 programmable current sources, which operates an array of 625 microelectrodes. Since the current source is in direct contact with the visual cortex and act as an interface between the operative part of the implant and the brain, a serious investigation should be made to find precisely the requirements for the ideal current source architecture. Many current source architectures have been proposed in the past to stimulate the bladder [4], [5], arms, legs and visual cortex [6] or even for high definition television applications [7].

In the present paper, a survey on current source architectures is elaborated to find the most appropriate choice for our application. A complete description of the selected design is also presented. First, considering the source is dedicated to be used in a fully implantable system, power consumption and integration area should be the most important parameters to minimize. Second, since the

stimulation strategies are not yet determined, the needed current source must allow flexibility to the implant by offering different signal (5-bit resolution) amplitude set with a programmable reference current. This specificity gives the possibility to adapt the right current level because the phosphenes threshold produced by electrical signals are not the same for different individual and the other reason is a possible insensitivity phenomenon with a long period of stimulation [1], [2]. In addition, the current source should not cause damage to the cortex. It should reduce glitches due to the switching of transistors and allow bipolar stimulation to minimize the charge accumulation in tissues.

In the remaining sections, different architecture types will be presented in section II. Then, the selection of an adequate current-source will be made in section III and the selected circuit will be presented in section IV.

II. DIFFERENT DAC ARCHITECTURES

Typically, a current-source module is composed of three major components such as a 5-bit digital to analog converter, an output controller and an electrodes selector (Fig. 1). The electrodes selector will be the subject of future work. In an other view, the output controller has to produce a bi-directional current stimulation to minimize charge accumulation in tissue. This task is done by an H architecture circuit based on Bourret's work [5], which is controlled by simple logic gates. A current mirror can also be added if current multiplication is needed. Finally, the DAC has to restore the digital signal. Since there are several Nyquist-rate DAC architectures possibilities to realize the current source, it is important to find advantages and inconvenient of each one. Basically, we can divide converters in two specific categories: voltage mode and current mode converters.

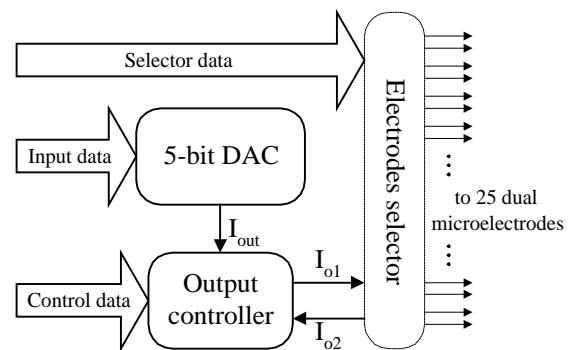


Fig.1: Block diagram of one current-source module

A. Voltage Division Converters

The voltage mode converter generates a voltage analog output signal. It requires in the basic model a resistor string to recreate different weighted binary voltage levels. A transmission gate system controlled by N-bit input word select the corresponding output voltage level. It takes 2^N resistors for N-bit resolution DAC. There are several variant of this architecture to reduce the number of resistance or to minimize large decoding network. However, in the present application it is essential to make voltage-current conversion with this model to avoid possible degradation of the source caused by the variation of the cortex impedance for different individual. This contributes to a more complex solution. Another disadvantage associated to this model is the permanent conduction of the resistor string that could badly affect our energy budget.

B. Current Division Converters

The basic current mode converter is composed of N binary weighted current source that produce the desired current level when activated. Each individual current source is realized with a single transistor with a binary weighted gate dimension ratio. This type of converter was used by Sawan [8] in the early prototype of a bladder stimulator implant. The problem associated with this architecture is the sensibility caused by layout mismatch and process deviation. Since converter performances depend on the most significant bit (MSB) accuracy, an error on the MSB transistor could deteriorate performances.

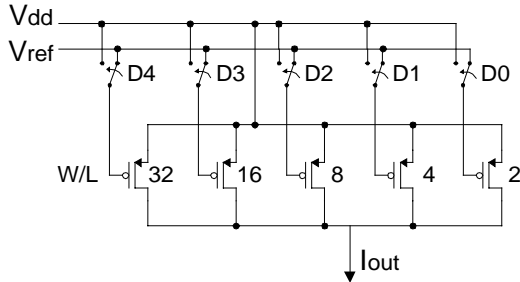


Fig. 2: A 5-bit version of the binary weighted current source DAC.

A variation of the previous architecture is to realize each individual current source with identical transistor (same gate dimension) placed in parallel or in series to deliver a pre-programmed binary weighted current level. The operation mode of this structure is basically the same of its predecessor. However, this architecture is less sensitive to fabrication process errors since the most significant bit current sources are made with several transistors randomly connected on the substrate considering the large number law. It is possible to reduce transistors error matching due to irregular electrical properties of the wafer by using common-centroid geometry layout technique. St-Amand *et al.* [4] and Bourret *et al.* [5]

used this architecture in their programmable current source dedicated to bladder stimulation implant.

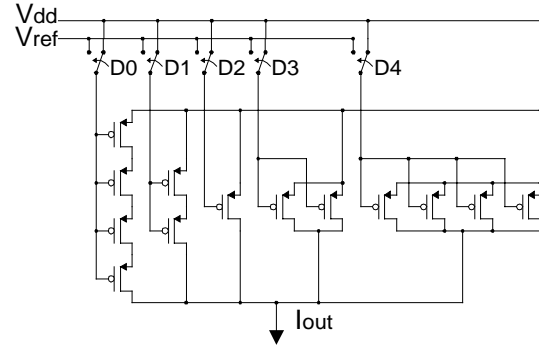


Fig. 3: A 5-bit version of the binary weighted current source DAC made with identical P type transistors.

Another architecture of digital to analog converter consist to digitally encode the binary weighted input value to a thermometer-code equivalent. This gives a digital-to-analog converter made of 2^N identical current-sources with the same binary weight for a N-bit resolution. It has the advantage of a low differential nonlinearities (DNL) error and a guaranteed monotonicity since all individual current-sources are identical. Moreover, it is possible to reduce glitching noise by using latches for the thermometer code and considering that each current source has the same switching delay. Unfortunately, the number of elements required by this structure grows exponentially and the complexity of the decoding logic increases with the degree of resolution.

Finally, the last current mode digital to analog converter class is the ladder architecture DAC or more specifically the R-2R ladder converter. This model operates like the binary weighted current-sources structure except that the current is scaled with resistance ladder. This gives a surface expensive and a non-energy efficient circuit since the resistance ladder is always conducting.

III. SELECTION OF THE ADEQUATE CIRCUIT

The previous section showed different alternatives to realize the programmable current-source. Considering most important criteria for our application such as energy and surface efficiency, structure made with resistance can be rapidly eliminated. Since less sensitive approach to process deviation is preferred, binary scaled current source made with identical transistors and thermometer code-based converter architectures are the only two possibilities remaining. The first one is a simple and a surface efficient structure while the other one is able to minimize glitch area and DNL error. On the other hand, it is possible to satisfy the second requirement of creating different current amplitude ratio and current level to allow flexibility to the implant with both remaining possibilities. However, the last criteria consisting of providing a safe and a reliable implant could be accomplish

only by a thermometer code based converter particularly if we want to minimize glitch area. In this case, the problem is to try to keep benefits offered by this architecture without the disadvantage of large number of components and complex decoding logic.

A possible solution is to propose a modified thermometer-code-based digital to analog converter where only the most significant binary part is transformed to a thermometer code equivalent since this part contribute the most in glitch intensity. The least significant part remains binary coded. Depending on the selected ratio of the least significant section, it is possible to reduce the number of element and simplify the decoding logic.

IV. CIRCUIT DESCRIPTION

Since our application requires to stimulate biological tissues, a 5-bit resolution is supposed to be sufficient. As mentioned at the beginning, stimulation strategies are not yet determined. The maximum output current should be as low as possible to not cause damage to the visual cortex and the minimum current should be high enough to produce phosphenes. Then, the programmable current source must be able to generate several signal shapes with different amplitude ratio indicated by the binary encoded equivalent. The simplified schematic of one current source is presented in figure 4 with all controlling digital inputs. Identification of these control signals is presented in table 1 and the different available current levels are shown in table 2.

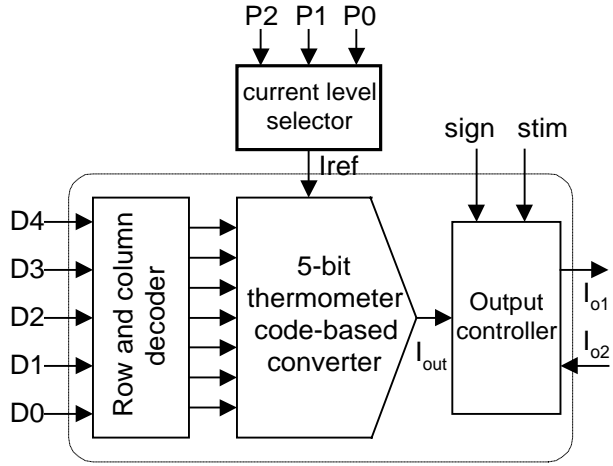


Fig. 4: Simplified diagram of a programmable current source

Table 1: Control signals identification

Signals	Functionality
D4 - D0	Binary encoded amplitude current ratio
P2 - P0	Binary encoded minimum current level
Stim	Current source activation
Sign	Current direction in the electrode

Table 2: Available current levels

Selected current level (P2 P1 P0)	Current reference level Iref (uA)	Maximum output current (uA)
111	4.00	124.0
110	3.42	106.0
101	2.85	88.5
100	2.29	70.8
011	1.71	53.1
010	1.14	35.3
001	0.57	17.7
000	0	0

The proposed current-source block diagram is shown in figure 5. It contains a simplified 4-bit row and column decoder for a thermometer code-based DAC developed by J.H. Kim *et al.* [7]. It is composed of 15 identical 2-LSB current sources to form a 4-bit thermometer code converter for the most significant part. The remaining part is a binary encoded 1-LSB current source to finally give a 5-bit DAC.

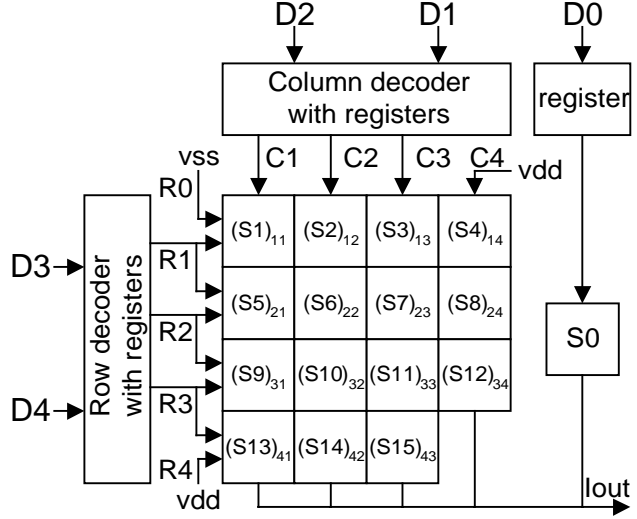


Fig. 5: Block diagram of the proposed 5-bit DAC with row and column decoder

Individual 2-LSB Current Source

Each individual current-source is a simple current mirror made with two identical N type transistors (Q_{2a} and Q_{2b}) in parallel to have a resulting current twice the reference current value. The cell, showed in figure 7, is controlled by a switching decoder with R_i , R_{i-1} and C_j signals. Those signals are generated by the column and the row decoder demonstrated below. The selector is a customized logic gate where the logic output G_N is defined by the equation:

$$G_{i,j} = (\bar{R}_i + \bar{C}_j) \cdot \bar{R}_{i-1} \quad \text{for } i,j = 1,2,3,4$$

The remaining 1-LSB current-source S0 is similar to the others except that the current mirror is made of only one transistor and the gate selector is not required.

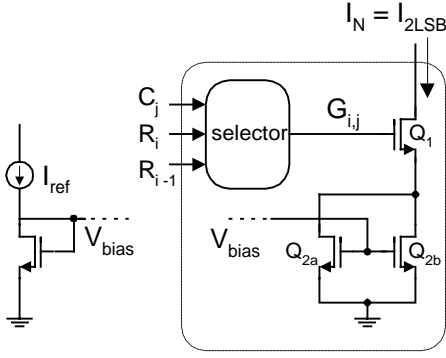


Fig. 6: An individual current source with the corresponding bias circuitry

Row and Column decoder

The row and the column decoder (Fig. 7) are a simple digital circuit made with basic logic gate such as an inverter, a NOR-gate and a NAND-gate. Basically, it converts the binary code to its thermometer code equivalent.

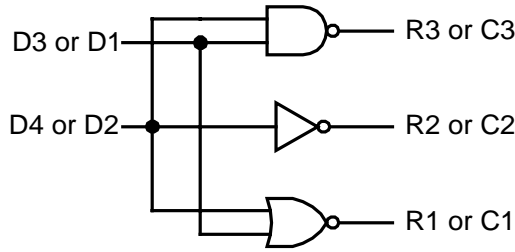


Fig. 7: Logic diagram of the row and column decoder

The proposed current-source has been designed and simulated with the Cadence Analog Artist tool using the CMOS 0.35 μ m technology from TSMC. An analysis has been made with the solution based on St-Amand's architecture [4] in order to compare the obtained performances. Those results are presented in table 3.

Table 3: Comparison between architecture

Architecture	Thermometer code-based converters	Binary weighted current DAC with minimum size transistors
Resolution	5 bit	5 bit
Max. power consumption	< 1 mW	< 1 mW
INL*	0.05 LSB	0.67 LSB
DNL*	0.04 LSB	0.18 LSB
Number of elements	157 transistors and 7 registers	45 transistors and 5 registers
Complexity	Medium	Low

* represent the worst case of the different current levels

V. CONCLUSION

A 5-bit modified thermometer code-based digital to analog converter has been presented. Since reliability, flexibility and power consumption were important parameters to overcome, the proposed current source is the most appropriate choice for our application. It has been selected between different possibilities to closely satisfy the criteria. The presented current-source architecture is a little more complex than the binary weighted current DAC with minimum size transistors. However, this is an adequate compromise between cost and performance since glitch presence has to be reduced. The fabrication of the proposed current-source is undertaken. Future developments include the design and the fabrication of the complete implantable visual microstimulator with the electrode array.

VII. ACKNOWLEDGMENTS

Authors would like to acknowledge the financial support of this project from the Natural Sciences and Engineering Research Council of Canada (NSERC) and Micronet.

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