

Temperature dependent leakage sensors using specially designed DRAM cells

ECE658 VLSI Design Final Project

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Abstract : The DRAM cells consist of one or several MOSFET devices and the subthreshold leakage current through the MOSFET strongly depends on the temperature variation. Therefore, it is obvious that the leakage of a memory cell is highly related to temperature variation. The temperature of the circuit can be measured indirectly by using leakage sensors which can be applied to various VLSI circuits because of its small size and compatibility. Motivated by the thermal sensitivity of the MOSFET and the circuit devices, we studied leakage based thermal sensors in different technologies such as 130nm, 65nm and 45nm and 3 types of leakage devices from MOSFET to the circuit. First, we showed the IV characteristics and the subthreshold leakage current through each MOSFET. Then, we tried to find out how the subthreshold leakage current through the MOSFET make the leakage sensors possible. Finally, we obtained the plot for leakage and temperature, the power consumptions, areas and noise immunity for each leakage devices.

1. Introduction

The increase in the needs of the high functional and high performance VLSI design has produced an increased in complexity and in number of transistors. In spite of current low voltage operating circuit, the power consumption has also increased and that has brought thermal issues [6]. It has been reported that the operating temperature of most current complex chip is over $70^{\circ}C$, and it is even over $130^{\circ}C$ in some case. Thus, careful thermal management is one of essential part of low power consumption and reliability of the circuit.

Many types of thermal sensors have been proposed successfully. However, the common problems of the most of them are too big and power hungry and thus restricting their usage for the various designs [5]. And some of them are needed a special process to be implemented in a die. For example, thermal sensors based on diode which is adopted in PowerPC have a merit such as the immunity of power supply noise but it is very difficult to be implanted into the normal cell based design [5].

We studied the leakage based thermal sensors based on the leakage current and temperature relationship. We can measure the temperature in the chip indirectly by measuring the leakage current because the leakage current of the transistor is highly related to temperature.

$$I_{leakage} = ke^{-qV_{th}/(K_B T)}$$

where the q and K_B are physical constants, a and k are device parameters and T is an absolute temperature [5]. As we can see, the sub-threshold leakage current is related to threshold voltage V_{th} and a temperature. Therefore, if we can minimize the effect of the V_{th} , the measured temperature will be reliable.

However, direct measurement of the leakage current device is inefficient and expensive to measure the temperature. Instead, a voltage comparator is relatively small, cheap and easy to implement compared to the leakage current measurement device. Therefore, we can think of another way to measure the temperature in the circuit by measuring the voltage drop because the leakage current is proportional to the voltage drop in time,

$$I_{leak} = C \frac{dV}{dt}$$

where the C is a capacitance of transistor and dV/dt represents voltage drop caused by leakage current.

There are many advantages using leakage based thermal sensors. It is small, low power consumption, and can be easily adapted to various technologies [5]. In this study, we try to test 3 types of specially designed DRAM cell which are optimized for the leakage device. By studying these, we can expect to find the most suitable leakage based thermal sensor for the specific circuit.

2. Device Characteristics

The temperature dependent leakage sensors using DRAM cells basically consists of one or several MOSFETs which implies that the characteristics of leakage sensors strongly rely on the MOSFET devices. Motivated by the strong dependence on the MOSFET characteristics, we first try to find out how the subthreshold leakage current through the MOSFET changes with temperature in different technologies. However, extracting the subthreshold leakage current from HSPICE model is not that simple to do because we can not simply quantify the leakage current from I-V characteristics by HSPICE simulation. Therefore, we

need to extract some device information from the HSPICE model card such as oxide thickness, doping profiles, threshold voltage and so on. Then we need to calculate the leakage current based on the drift-diffusion model by hand or computer.

For this purpose, we programmed leakage current simulator by FORTRAN90 which calculate the subthreshold leakage current through the each NMOS in different technologies as temperature changes. The analytical expressions for the subthreshold leakage current can be obtained from BSIM4 manual [1][2].

The subthreshold leakage current I_{ds} is

$$I_{ds} = I_0 \left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right) \right] \exp\left(\frac{V_{gs} - V_{th} - V_{off}}{nv_t}\right) \quad (1)$$

where the $v_t = k_B T / q$ is a thermal volt, V_{th} is a threshold volt, n is a subthreshold swing and I_0 is

$$I_0 = \mu \frac{w}{L} \sqrt{\frac{q \epsilon_{si} NDEP}{2 \Phi_s}} v_t^2 \quad (2)$$

where w and L is a channel width and the length, respectively and μ is a channel mobility.

The threshold volt V_{th} is given by

$$V_{th} = VTH0 + \delta_{NP} (\Delta V_{T,BodyEffect} - \Delta V_{T,ChargeSharing} - \Delta V_{T,DIBL} + \Delta V_{T,ReverseShortChannel} + \Delta V_{T,NarrowWidth} + \Delta V_{T,SmallSize} - \Delta V_{T,PocketImplant}) \quad (3)$$

where the each component of the equations are described in [2].

The subthreshold swing n is

$$n = 1 + NFACTOR \frac{C_{dep}}{C_{oxe}} + \frac{C_{dsc_Term} + CIT}{C_{oxe}} \quad (4)$$

and the effective mobility is given by

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \times V_{bseff}) \left(\frac{V_{gseff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gseff} + 2V_{th}}{TOXE} \right)^2} \quad (5)$$

[1][2]. All capitalized parameters can be obtained from the HSPICE model card in different technologies.

The subthreshold leakage current can now be obtained by simulation based on the above shown essential equations even though we do not show very detail.

2.1. I-V Characteristics

The I-V characteristics are generated by HSPICE simulation for different technologies. As we can see the Figure 1-3, the source to drain current in unit length decreases and the subthreshold leakage current increases as the channel length decreases. Compared to the published data [4], the IV characteristics shows a different aspects. The on current is supposed to be greater in short channel length device regarding to [4]. However, in our simulation this aspect is opposite and we do not figure out why for now.

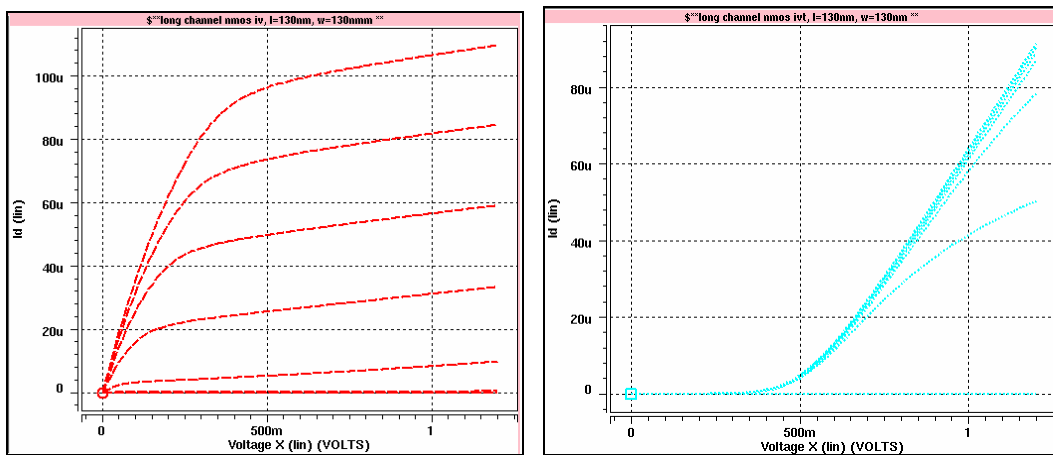


Figure 1 : 130nm NMOS IV (left), IVT (right) characteristic

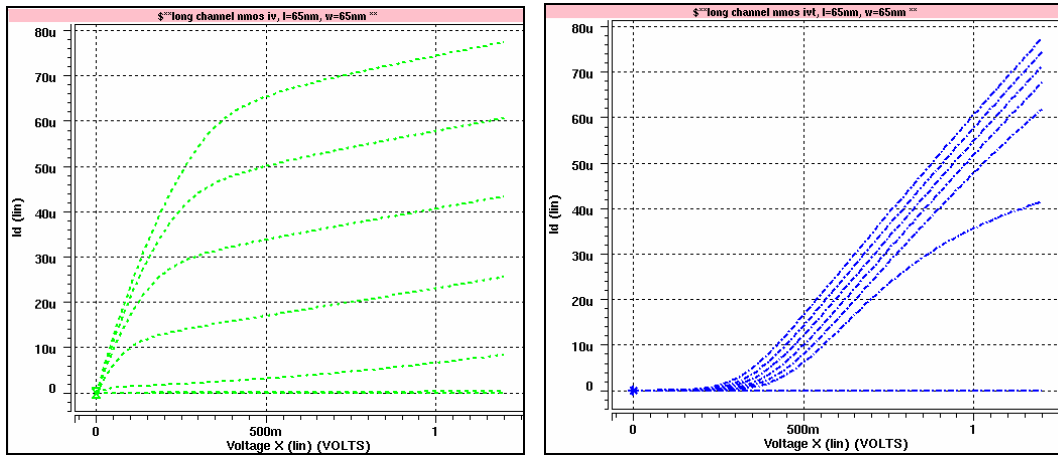


Figure 2 : 65nm NMOS IV (left), IVT (right) characteristic

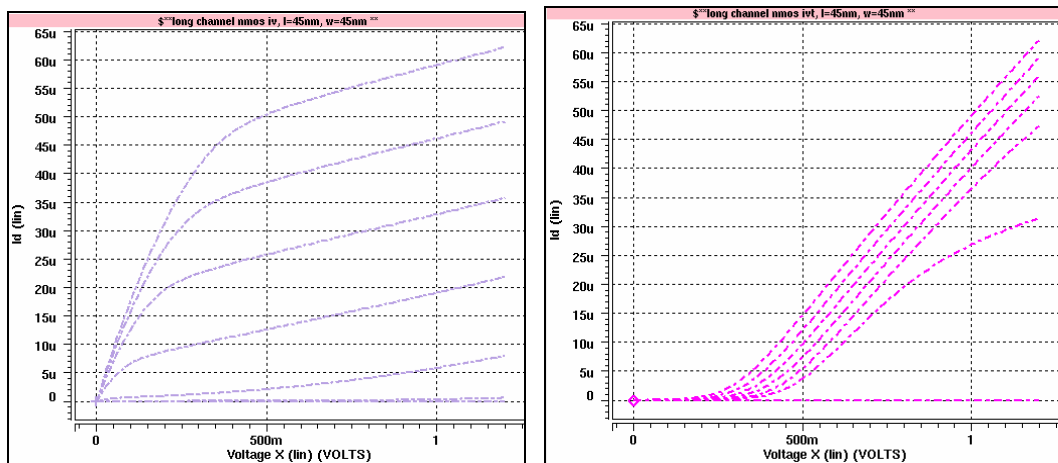


Figure 3 : 45nm NMOS IV (left), IVT (right) characteristic

2.2. Subthreshold leakage current

In order to obtain the subthreshold leakage current, we need to extract some information of the MOSFETs for different technologies. The necessary information of the devices can be obtained from the HSPICE model card and then the leakage current can be numerically calculated by FORTRAN simulation. The simulation code is shown in Appendix A.

In figure 4-6, we simulated the subthreshold leakage current through the NMOS in different technologies, i.e. 130nm, 65nm and 45 nm. As we can easily see, there is not a major difference in leakage current by changing the source-drain voltage and the leakage current linearly increases as the temperature increases. In Figure 4., the leakage current for 130nm NMOS is approximately 0.3nA at an operating

temperature around 80 °C which is slightly larger than 65nm and 45nm. And also, in Figure 5. the 65nm NMOS shows a larger leakage current than 45nm. Therefore, we can conclude that the leakage current through the NMOS is getting larger as the channel length of the NMOS increases which are shown in Figure 7. This result shows a good agreement with already published data [3] and thus we can expect that the voltage change in the DRAM cells which consists of one or several NMOS is faster in larger channel length device, i.e. 130nm NMOS.

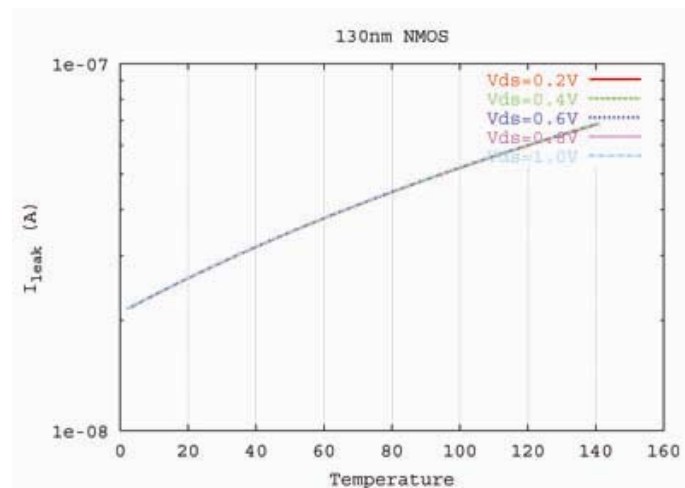


Figure 4 : The subthreshold leakage current in 130nm NMOS. The leakage current is approximately order of 10^{-7} to 10^{-8} (A) and does not change much in different drain-source voltage.

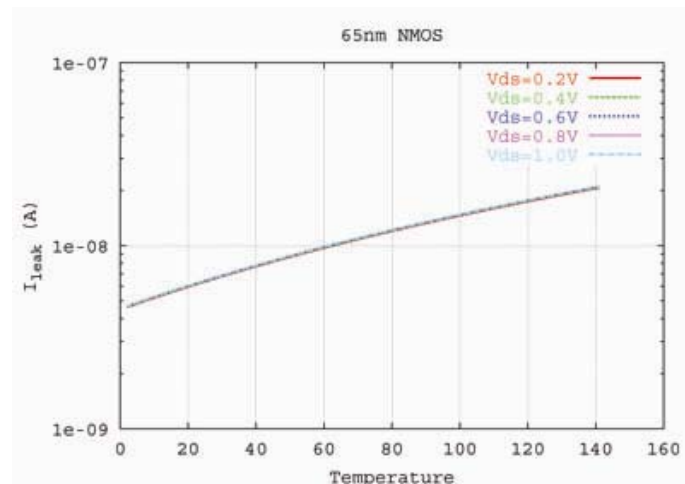


Figure 5 : The subthreshold leakage current in 65nm NMOS. The leakage current is approximately order of 10^{-7} to 10^{-9} (A) which is slightly less than 130nm NMOS .

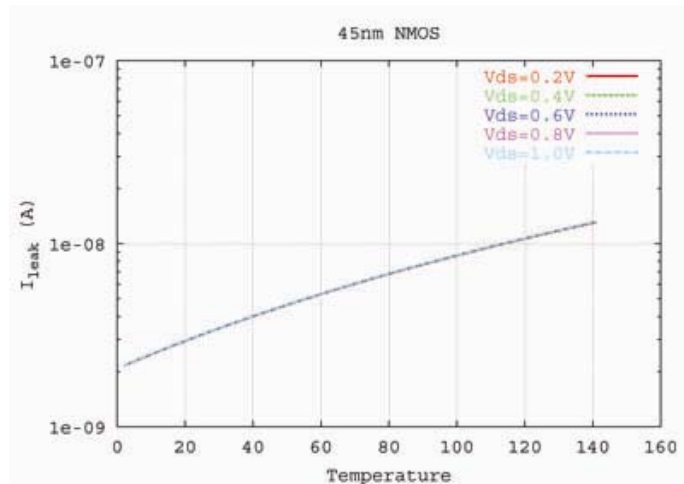


Figure 6 : The subthreshold leakage current in 45nm NMOS. The leakage current is approximately order of 10^{-8} to 10^{-9} (A) which is the smallest among the above compared devices.

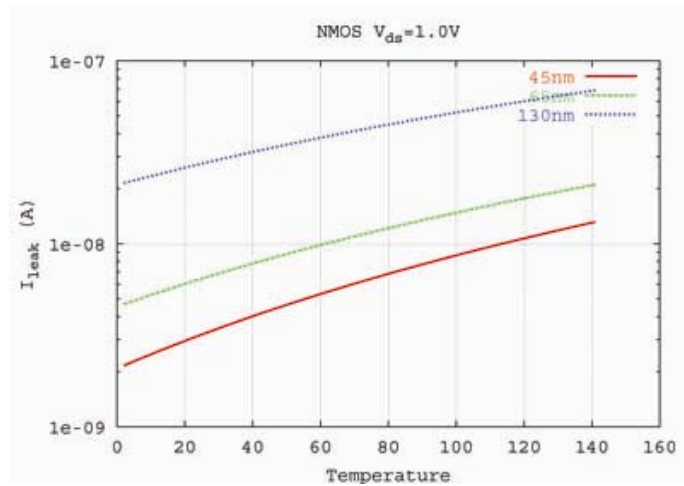


Figure 7 : The subthreshold leakage current for different technologies are compared at a fixed drain-source voltage $V_{ds}=1.0V$. The long channel device, $L=130nm$, shows the largest leakage current and the short channel device, $L=45nm$, shows the smallest leakage current.

3. Leakage sensor

Figure 8. shows a leakage sensor structure we designed. When we give the 'enable' signal, the leakage device would begin to be charged and simultaneously the 'sensing' pulse would be transferred to voltage comparator. The output voltage of the leakage device decays from high to low and eventually would approach to reference voltage(V_{ref}) level, then the output of the voltage-comparator starts to be oscillated due to the interference with 'sensing' pulse and moves to high voltage level. However, the oscillating output voltage from the voltage comparator is highly unstable, thus we need to stabilize the output signal with help of the buffer.

The above shown specially designed leakage sensor is very compatible because the only thing we need to do is to change the leakage device for various purposes. In addition, the sensor is composed of only MOSFETs and thus this can be implemented by the general MOSFET technologies.

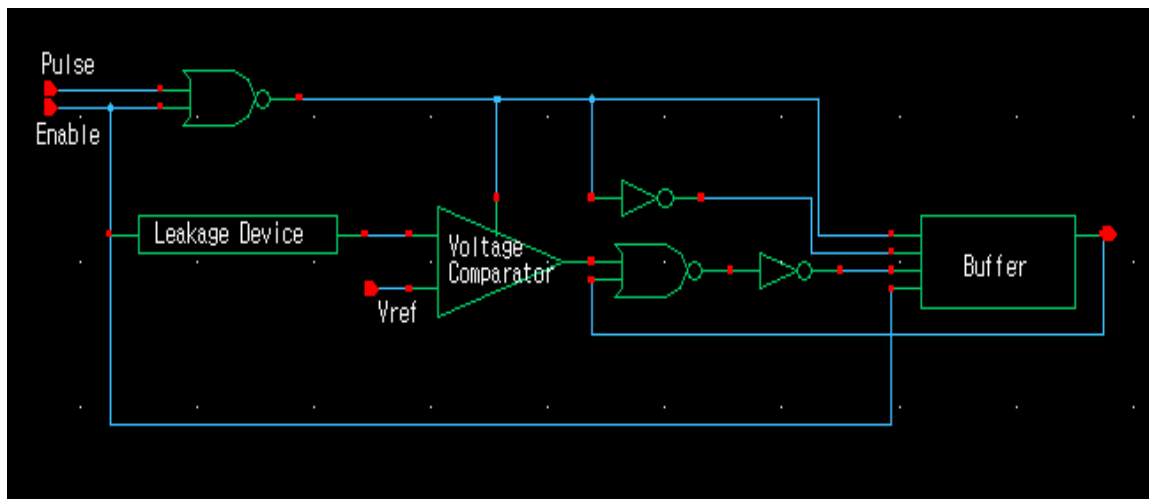


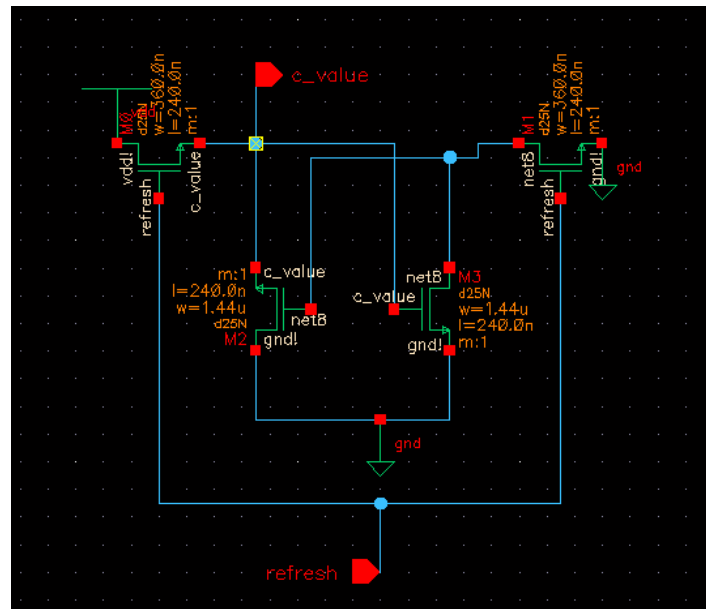
Figure 8 : Schmetic of Leakage sensor

3.1. Leakage devices

3.1.1. 4T DRAM Cell

The first leakage device for the leakage sensor is the 4T DRAM cell shown in Figure 9. (left) which is from [5]. As we can see, the 4T DRAM cell is basically the SRAM cell without the PMOS and consists of only 4 NMOS which are connected to give a positive feedback which would cause the fast charging speed.

Figure 7. (right) shows the voltage decaying characteristic due to the leakage current in time. Thus, we can indirectly measure the temperature by measuring the voltage drop in the circuit.



Voltage

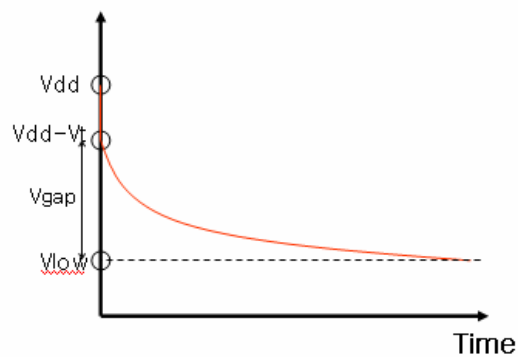


Figure 9. 4T DRAM Cell [5]

In order to obtain an accurate temperature with the 4T DRAM cell, we need to have a nice voltage decaying curve by eliminating a side effect such as the leakage current from the T2. However, the leakage current from T2 never be decayed completely because T2 is connected to V_{dd} , as we can see in Figure 9. (right). Therefore, the size of T2 should be minimized and T1 should be big enough. In this study, the size of the T2 is minimized and T3 is 8 times bigger than T2.

And also, the voltage high of the T1 is not equivalent to V_{dd} because T2 is a pass transistor which has $V_{dd}-V_{th}$ as a high voltage level. This lowered voltage high of the T1 makes a small V_{gap} which finally results in difficulties in accurate measurement of the temperature.

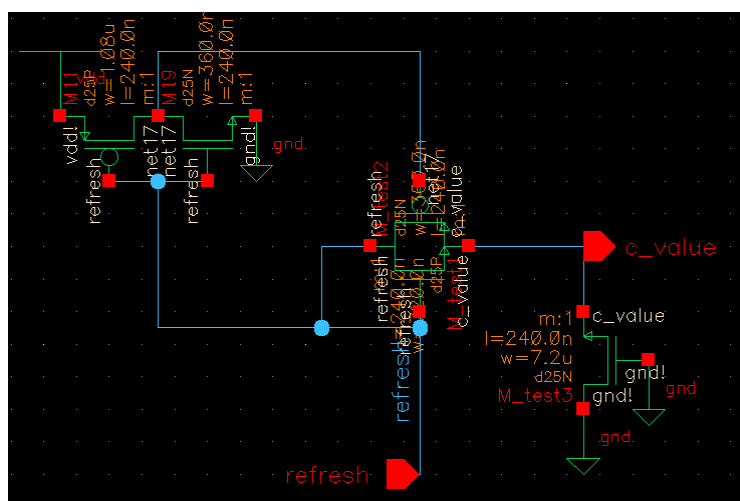
In addition to the lowered V_{gap} , the reference voltage V_{low} and the threshold voltage V_{th} is varied by temperature variation. Therefore, it is difficult to determine the starting voltage and ending voltage for decay measurement. However, the advantage is still held because 4T DRAM cell has fast charging speed due to its positive feedback [5].

3.1.2. 1T DRAM Cell with transmission gate

The second leakage device for the leakage sensor is the modified 1T DRAM cell shown in Figure 10. The 1T DRAM cell usually consists of only one NMOS but in this study we modified the 1T DRAM cell circuit structure to obtain proper voltage decaying characteristics for a leakage based thermal sensor. The major modification is that we include the transmission gate and inverter so that the leakage current can not flow from T2 to T1 in decaying period which results in enough V_{gap} in Figure 10 (right).

In this circuit, the explicit capacitance is not included in the 1T DRAM cell which results in short decaying time. Therefore, at least we need the enough V_{gap} to compensate the short decaying time so that we can accurately measure the decaying time. But we do not need to worry about the enough V_{gap} because this circuit has rail to rail decay which automatically guarantees the maximum and fixed V_{gap} .

There are a pros and cons to have a short decaying time compared to the 4T DRAM cell in this circuit. The disadvantage is that we have low accuracy in high temperature but the advantage is that we can repeatedly measure the temperature variation in the circuit with high resolution.



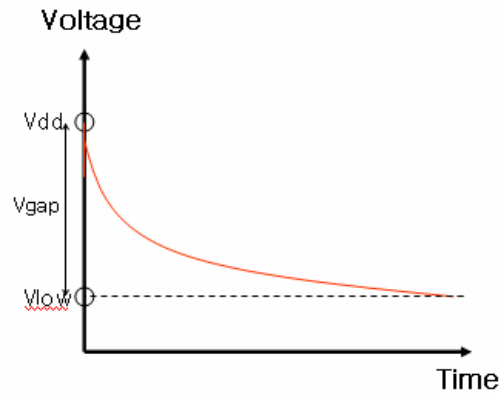


Figure 11. 3T DRAM cell with transmission gate

The last leakage device we tried for the leakage sensor is a modified 3T DRAM cell shown in Figure 11. In this circuit, we eliminated some unnecessary components in 3T DRAM cell for leakage measurement. Instead, we added a transmission gate and an inverter same as the 1T DRAM cell but the gate of the T1 is connected to the transmission gate T2 in this circuit contrast to the 1T DRAM cell.

The voltage drop characteristic in Figure 11. (right) shows a relatively long decaying time compared to the 1T and 4T DRAM cell due to the gate capacitance of T1. And also, the slope of the voltage drop curve is smooth so that the small variation in voltage drop causes large variation in decaying time. In other words, this DRAM cell is largely affected by the supply noise compared to other leakage devices. In addition, we have a high accuracy at one time measurement but low resolution at many time measurements.

3.2. Voltage Comparator

In order to implement the leakage based thermal sensor, we need to check if there is enough voltage drop come along with the leakage current. In other words, the coincidence should be happened between the decayed voltage and the reference voltage at the same time. In this case, the reference voltage should be greater than V_{low} .

We can use the sense amplifier as a voltage comparator shown in Figure 12. The Bit signal is connected to the leakage device and the Bit-Bar signal supplies the reference voltage. If the Bit and Bit-Bar signals approach to the same low voltage level, the output would approach to the V_{dd} . Therefore, we can determine if there is enough voltage decaying of the leakage device.

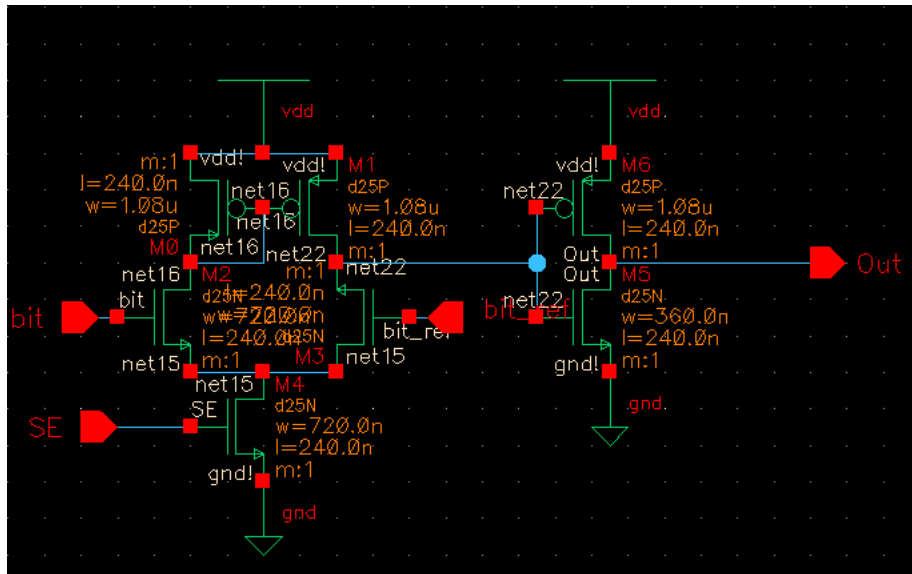
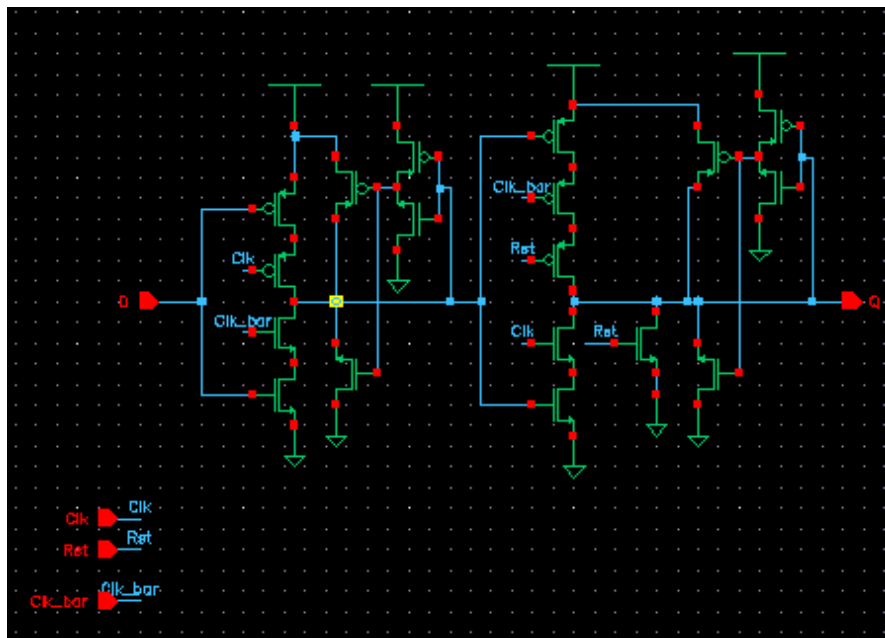


Figure 12. Voltage comparator using sense amplifier

3.3.3. Buffer



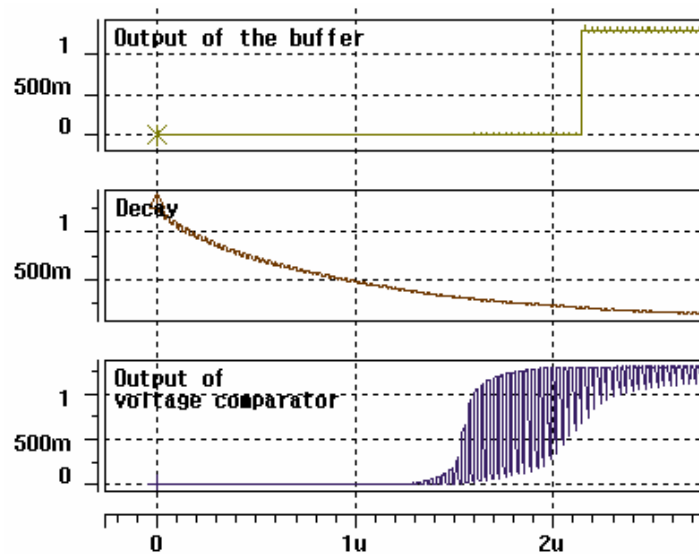


Figure 13. C2MOS D-FF with keeper for buffer

The output of the voltage comparator is not a nice square wave form because of the sense enable pulse which makes the output oscillated. If the frequency of the sensing pulse increases, the output of the sense amplifier begins to oscillate when the output goes to high. This interrupts the proper operation of the timing device such as a counter connected to the sense amplifier.

The buffer shown in Figure 13. consists of 1 D-FF and the logic which feedback D-FF's output to the AND gate. The main function of the buffer is to make stable the unstable output of the sense amplifier. We use the C²MOS logic style to implement the D-FF in this study. And also, we add a keeper because the unexpected error happens when there is no change in stored value for a long time in C²MOS.

4. Data

In this study, we compare the characteristics such as decaying rate, noise immunity, power consumption of the three different leakage devices shown in section 3. First, we simulated the voltage decaying rate due to the leakage current as the temperature changes because if we know the voltage decaying rate for the different technologies, we can determine the temperature of the circuit. Second, we simulated noise immunity of the voltage decaying rate with the temperature for the different technologies and different leakage devices. In a real circuit, there always exists unexpected supply noise which makes significant errors on measuring the temperature. In general, it is known that the voltage decaying rate is very sensitive on the supply noise [5]. Third, we change the width of the NMOS in the leakage device.

4.1. Sensor's characteristic with temperature

In this section, the voltage decaying rate is simulated as the temperature increases. As we already shown, the voltage decaying in time is proportional to the subthreshold leakage current of the MOSFET devices and the leakage current increases as the temperature increases. For this reason, we can expect that the voltage decaying time would be short as the temperature increases.

Figure 14. shows that the voltage decaying rate vs temperature for different technologies and different leakage devices. The 1T DRAM cell leakage device shows the fastest voltage decaying rate among the three of the leakage devices and the 3T is the slowest due to the large gate capacitance. And also, the decaying rate for the 45nm NMOS leakage device is the slowest for the 4T and 1T DRAM cell. This is obvious because the leakage current of the 45nm is the smallest compared to the 130nm and 65nm NMOS. However, this tendency does not agree with the 3T DRAM cell leakage device because the 3T DRAM cell uses the gate leakage current instead of the subthreshold leakage current which is much larger than the gate leakage current. Thus, the reason for the slow voltage decaying rate of the 3T DRAM cell compared to the 1T and 4T DRAM cell is a smaller gate leakage current than the subthreshold leakage current of the 1T and 4T DRAM cell.

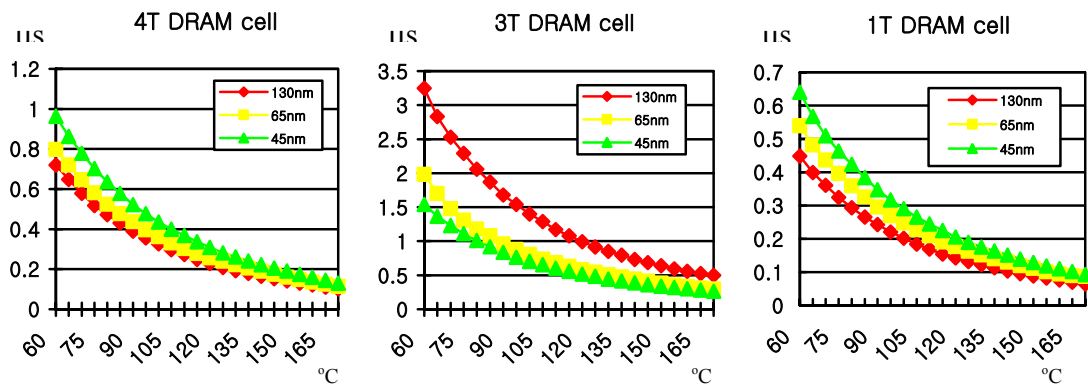


Figure 14. Decay time VS Temperature

4.2. Supply noise immunity

It is generally known that the voltage decaying rate is very sensitive on the supply noise at low temperature but at high temperature. Motivated by the sensitivity on the noise at low temperature, we show how the supply noise affects the voltage decaying rate for different leakage devices. In this study, we change the supply voltage V_{dd} +10 and -10% of the normal operation.

In Figure 15. and 17., the 4T and 1T DRAM cell show less than 2% discrepancy compared to the normal operation at high temperature for all different technologies. Thus the 4T and 1T DRAM cell is reliable for a temperature measurement because the usual operating temperature of the CMOS circuit is around 80°C. However, as we can see in Figure 16., the 3T DRAM cell is very sensitive on the supply noise around 80°C which implies that the temperature measurement of the circuit using 3T DRAM cell is not reliable. Thus, the 3T DRAM cell leakage device is not recommendable for the temperature measurement.

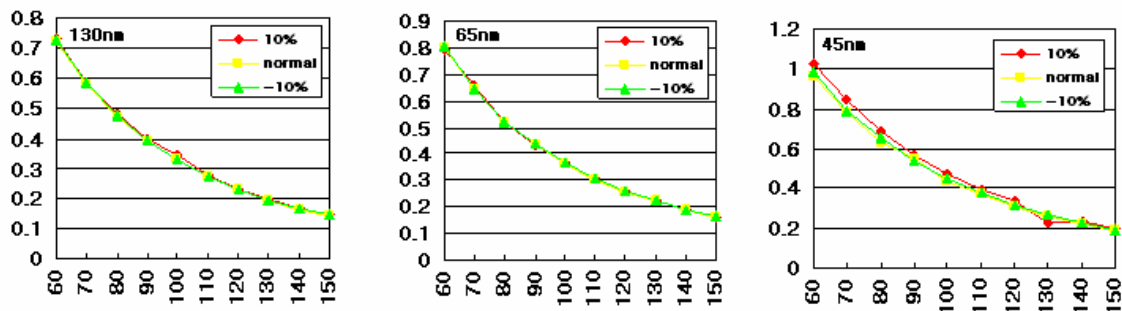


Figure 15. Noise immunity of 4T DRAM cell

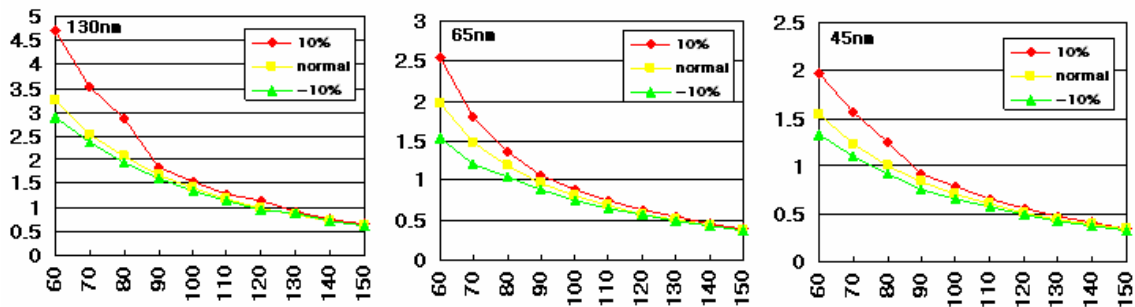


Figure 16. Noise immunity of 3T DRAM cell

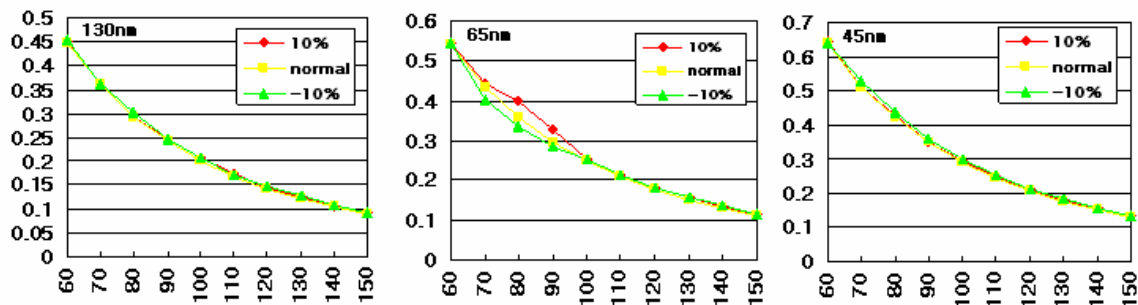


Figure 17. Noise immunity of 1T DRAM cell

4.2. Sensor's characteristic with width of the MOSFET

In this section, we change the width of the MOSFET of the each leakage device to determine the optimal size of the MOSFET. We test total six W/L ratio for different technologies, i.e. W/L=20, 40, 80 and W/L=8, 18, 24 because the voltage decaying time of the 3T and 1T DRAM cell does not make significant difference in small W/L ratio. As we can see, the voltage decaying time decreases as the width of the MOSFET increases in 4T and 1T DRAM cell due to the increased subthreshold leakage current through the channel of the MOSFET. However, the 3T DRAM cell shows an opposite behavior to the 4T and 1T cell. As we mentioned earlier, the 3T DRAM cell leakage device basically use the gate leakage current instead of the subthreshold leakage current through channel. If we increase the width of the MOSFET in the 3T device, the gate capacitance becomes large which makes the charging and discharging time longer. In other words, bigger the width of the MOSFET in 3T device, longer the voltage decaying time.

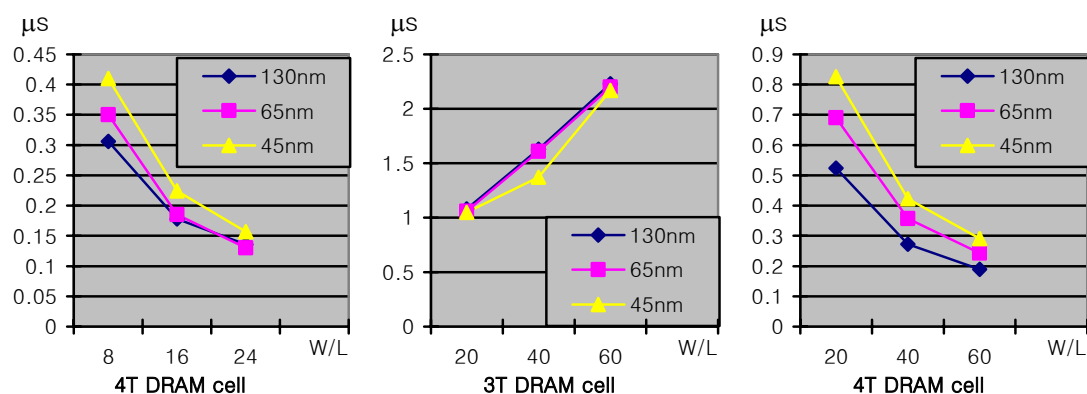


Figure 18. Decaying time VS Device size

4.3. Power consumption with sensing pulse frequency

The power consumptions of the each types of thermal sensor are shown in Figure 19. The most important role of the thermal sensor is the power management of a specific circuit which includes thermal sensor because the power consumption of the circuit is proportional to the temperature. Thus, it is obvious that the power consumption of the sensor itself should be small enough compared to the power consumption of the big circuit.

The power consumption of the thermal sensor strongly depends on the sensing frequency of the voltage comparator because we need a higher sensing frequency to measure the temperature accurately which consumes large power. Therefore, there is a tradeoff between the power consumption of the thermal sensor

and the sensing frequency. The strong dependences on the sensing frequency are shown in Figure 19. for different technologies. As we can see, the power consumption of the thermal sensor increases as the channel length of the MOSFET increases at fixed sensing frequency and also the power consumption of the 3T DRAM cell is larger than 4T and 1T DRAM cell in the whole range of the sensing frequency in the case of 45nm and 65nm channel length NMOS. However, the power consumption of the 1T DRAM cell is larger at a low sensing frequency when the channel length is 130nm. The reason for this phenomenon is not clear for now but still interesting.

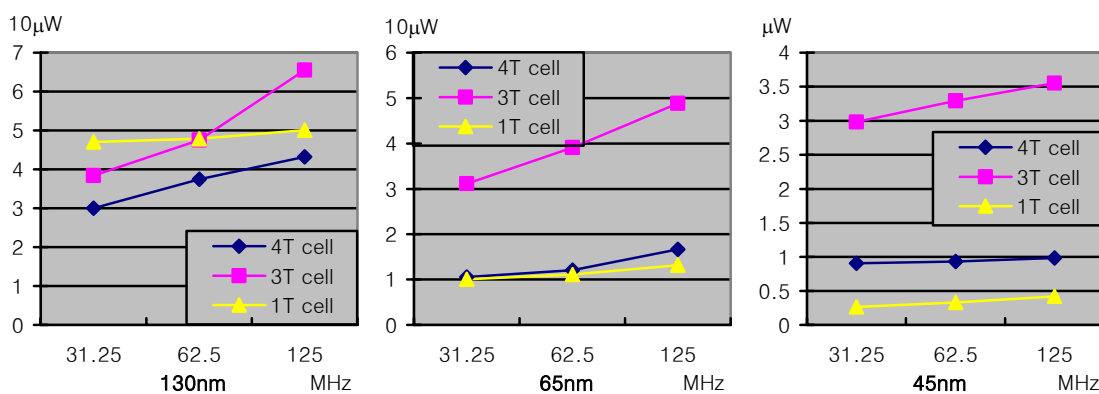


Figure 19. Power consumption VS Sensing frequency

5. Determination of the temperature

In order to determine the temperature of the circuit, we need to measure how long the voltage decaying from voltage high to reference voltage takes. To measure the decaying time, we devise the 16-Bit counter. The 16-Bit counter counts the sensing pulses which keep oscillating from voltage high to reference voltage. In this study, we only test the 130nm 1T DRAM to show how easily the temperature can be determined.

5.1 Leakage based thermal sensor with 16bit counter

The schematic of the thermal sensor in which the 16-Bit counter is implemented is shown in Figure 20. The counter will be reset when leakage device is charged by the enable signal. During the voltage decaying, it counts the number of sensing pulse and then the stored value of the counter is held when the voltage approaches to the reference voltage.

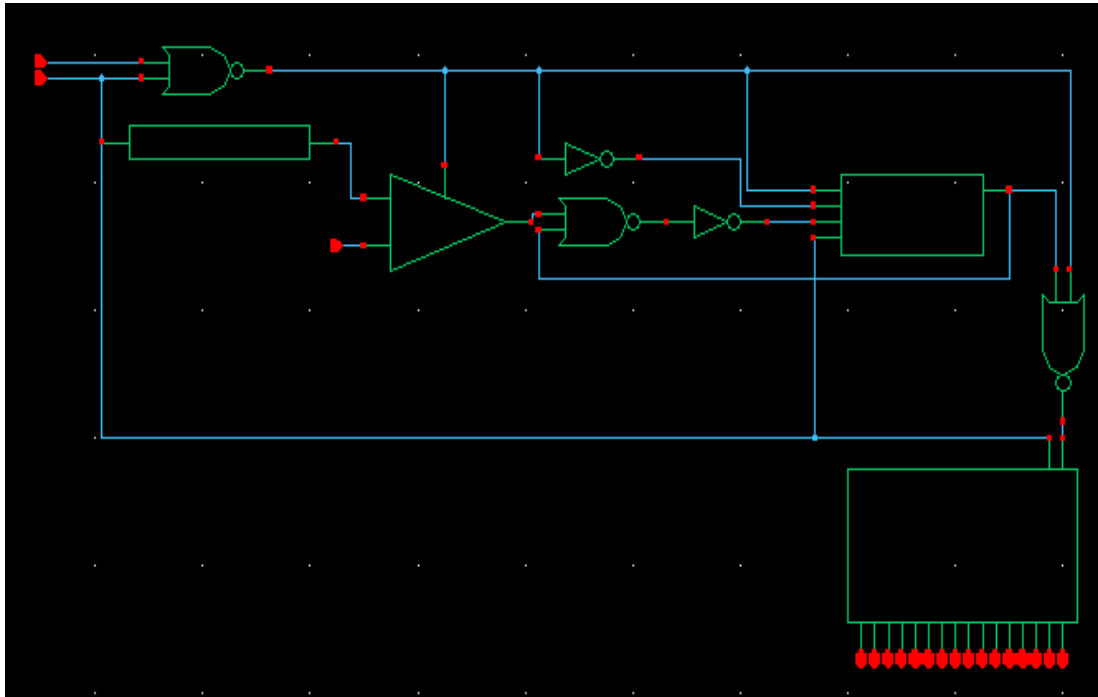


Figure 20. Thermal sensor with 16-Bit counter

5.2 wave form for the application.

Figure 21. shows the simulation result of the thermal sensor with 16-Bit counter. The waveform shown below is obtained by HSPICE simulation where the frequency of sampling pulse is $0.25\mu\text{s}$. The 'buf_out', a signal from buffer which latches the output of sense amplifier, automatically jumps to high when the voltage decaying approaches very close to the reference voltage. At last, the counter would stop counting and hold the final value.

In this simulation, the final stored value in the counter is '110011b' which corresponds to the specific temperature 80°C . The whole mapping table for the 'count' VS corresponding 'temperature' is summarized in Table 1. which has a similar result to the published data [5].

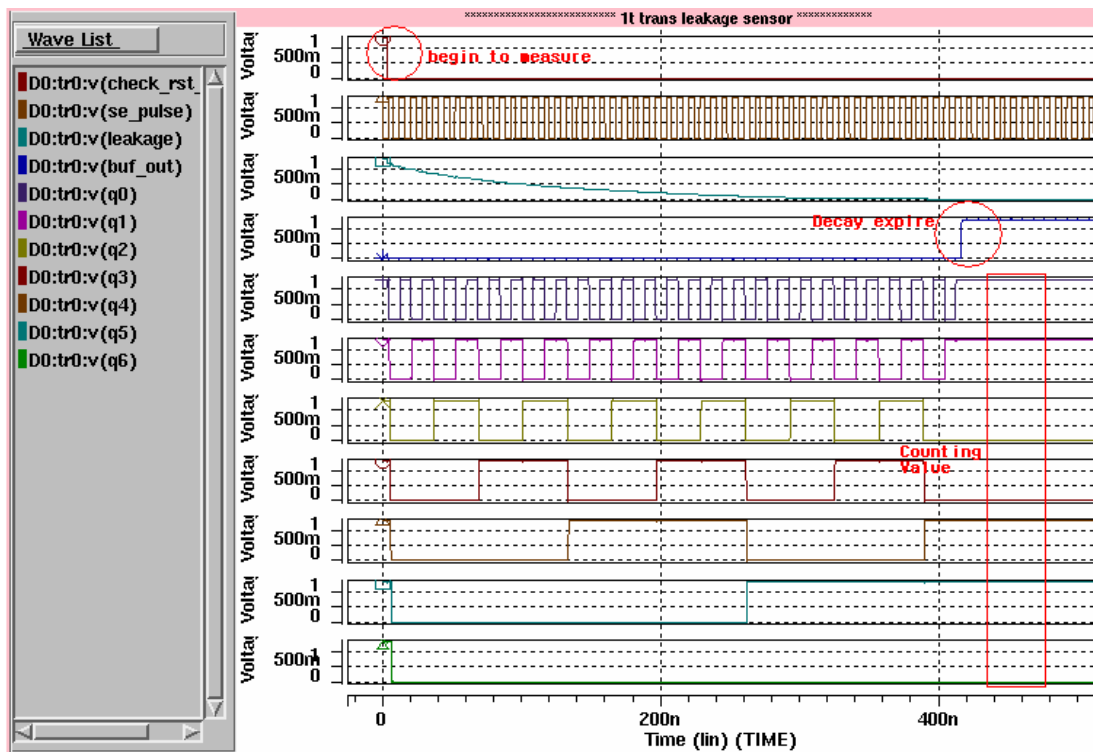


Figure 21. Simulation result of thermal sensor with counter

1T leakage sensor (130nm) Vref : 0.1V		
Temperature (°C)	count (binary)	count (decimal)
60	10010101	149
70	111100	60
80	110011	51
90	101100	44
100	100110	38
110	100001	33
120	11101	29
130	11010	26
140	11000	24
150	10110	22

Table 1. Mapping table with count and temperature.

6. Conclusions

Various leakage based thermal sensors are proposed and simulated in this study. The main idea of this study is that we can indirectly determine the temperature of the entire circuit by measuring the voltage decaying in time due to the subthreshold leakage current.

We numerically calculate the subthreshold leakage current based on the HSPICE model for three different technologies, i.e. 130nm, 65nm and 45nm NMOS. The leakage current through the MOSFET results in changing the voltage in time which makes the indirect measurement of the temperature possible. We verified that the large leakage current in large channel length NMOS causes fast voltage decaying in time which corresponds to the higher temperature.

Next, we propose the newly devised thermal sensors based on the 3T and 1T DRAM cell. In addition, we test the already published thermal sensor based on the 4T DRAM cell and then we compare the results from our device to the 4T DRAM cell. The major improvements of our 1T DRAM cell thermal sensor compared to the 4T DRAM are the small size, low power consumption and better accuracy to measure the temperature. And also, the benefit of using 3T DRAM cell thermal sensor is that we can have even better accuracy than 1T and 4T DRAM cell but it has larger power consumption and shows the very sensitive.

Future work

- Gate leakage current calculation through the NMOS and PMOS.
- Resolution measurement of the thermal sensor for reliability.
- Successive decay time differences of the various thermal sensor.

References

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Appendix A

FORTRAN 90 Source Code for Subthreshold Leakage Current Calculation

```
!ECE658 VLSI Design Final Project
!Leakage based thermal sensor
!Calculate the subthreshold leakage current through MOSFET
!Analytical expressions are from BSIM4 manual

!Started on Dec. 24, 2006
!Jiseok Kim

!130nm NMOS

Program main

Implicit none
!Device parameter
Double Precision, Parameter :: L=130.d-9, W=130.d-9

!physical constants
!kb(J/K), q(c)
Double Precision, Parameter :: kb=1.38d-23, q=1.6022d-19
!ni(m-3)
Double Precision, Parameter :: ni=1.45d16
Double Precision, Parameter :: ep0=8.854d-12, epsi=11.7*8.854d-12
Double Precision, Parameter :: pi=3.141592

!130nm NMOS
!HSPICE model parameter
Double Precision, Parameter :: K1=0.4d0, K2=0.01d0
Double Precision, Parameter :: TOXE=2.25d-9, TOXM=2.25d-9
Double Precision, Parameter :: NDEP=1.54d24, NSD=2.d26, PHIN=0.d0
Double Precision, Parameter :: W0=2.5d-6
Double Precision, Parameter :: XL=-60.d-9
Double Precision, Parameter :: EPSROX=3.9d0
Double Precision, Parameter :: DVT2=-0.032d0
Double Precision, Parameter :: NFACTOR=1.5d0
Double Precision, Parameter :: U0=0.05928d0, UA=6.d-10, UB=1.2d-18, UC=0.d0
Double Precision, Parameter :: MINV=0.05d0
Double Precision, Parameter :: VFB=-0.55d0, NGATE=2.d26
Double Precision, Parameter :: VOFF=-0.13d0, VOFFL=0.d0
Double Precision, Parameter :: VTH0=0.3782d0
Double Precision, Parameter :: LPEB=0.d0, LPE0=0.d0, DVTOW=0.d0, DVT1W=0.d0
Double Precision, Parameter :: DVT0=1.d0, DVT1=2.d0
Double Precision, Parameter :: K3=0.d0, K3B=0.d0, DSUB=0.1d0, ETA0=0.0092d0,
ETAB=0.d0
Double Precision, Parameter :: DVTP0=1.2d-10, DVTP1=0.1d0
Double Precision :: Klox, K2ox
!T=kelvin, Tcel=celcius
Double Precision :: PHIs, T, Tcel
Double Precision :: Vbc, Vbs, Vbseff, Vds, Vgs, Vpolyeff, Vpoly
Double Precision :: Leff, Weff
Double Precision :: Xdep, Xdep0, lt, ltw, lt0, vt
Double Precision :: Cox, Cdep
Double Precision :: n
Double Precision :: Ueff, Vgsteff, m, Vgse, Voff1
Double Precision :: I0, Ids(5,200)
Double Precision :: Vth, Vbi
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Double Precision :: Vth_body, Vth_rev, Vth_sm, Vth_DIBL, Vth_narr, Vth_char,
Vth_pock
Integer :: i,j,k

!main

!body-source volt
Vbs=0.d0
Vds=0.0d0
Vgs=0.2d0
Tcel=0.d0

Open(unit=10, file='sub_leak_130nm.data', status='replace')

Do j=1,5
  Vds=Vds+0.2d0
  Tcel=0.d0

  Do i=1, 200
    Tcel=Tcel+1.d0
    !temperature conversion. Input temperature would be in celcius
    T=273.15d0+Tcel

    vt=kb*T/q

    K1ox=K1*(TOXE/TOXM)
    K2ox=K2*(TOXE/TOXM)

    PHIs=0.4d0+(kb*T/q)*log(NDEP/ni)+PHIN

    !unit shold be checked
    Vbc=0.9d0*(PHIs-(K1**2.d0/(4.d0*K2**2.d0)))

    Vbseff=Vbc+0.5d0*((Vbs-Vbc-0.001d0)+Sqrt((Vbs-Vbc-0.001d0)**2.d0-
4.d0*0.001d0*Vbc))

    Leff=L+2.d0*XL
    Weff=W

    Xdep=Sqrt((2.d0*epsi*(PHIs-Vbseff))/(q*NDEP))
    Xdep0=Sqrt((2.d0*epsi*PHIs)/(q*NDEP))

    lt=Sqrt((epsi*TOXE*Xdep)/EPSROX)*(1.d0+DVT2*Vbs)
    ltw=Sqrt((epsi*TOXE*Xdep)/EPSROX)*(1.d0+DVT2*W*Vbs)
    lt0=Sqrt((epsi*TOXE*Xdep)/EPSROX)

    Cox=EPSROX*ep0/TOXE
    Cdep=epsi/Xdep

    n=1+NFACTOR*(Cdep/Cox)

    Vbi=(kb*T/q)*log((NDEP*NSD)/(ni**2.d0))

    Vth_body=(K1*TOXE/TOXM*Sqrt(PHIs-Vbseff)-
K1*Sqrt(PHIs))*Sqrt(1.d0+LPEB/Leff)-K2*Vbseff*TOXE/TOXM
    Vth_rev=K1*TOXE/TOXM*(Sqrt(1.d0+LPE0/Leff)-1.d0)*Sqrt(PHIs)
    Vth_sm=DVTOW*(Exp(-DVT1W*Weff*Leff/(2.d0*ltw))+2.d0*Exp(-
DVT1W*Weff*Leff/(2.d0*ltw)))*(Vbi-PHIs)

```

```

Vth_DIBL=(Exp(-DSUB*Leff/(2.d0*lt0))+2.d0*Exp(-
DSUB*Leff/(2.d0*lt0)))*(ETA0+ETAB*Vbseff)*Vds
Vth_narr=(K3+K3B*Vbseff)*TOXE/(Weff+W0)
Vth_char=DVT0*0.5*(Vbi-PHIs)/(Cosh(DVT1*Leff/lt)-1.d0)
Vth_pock=n*vt*log(Leff/(Leff+DVTP0*(1.d0+Exp(-DVTP1*Vds))))

Vth=VTH0+Vth_body-Vth_char-Vth_DIBL+Vth_rev+Vth_narr+Vth_sm-Vth_pock

!print *, 'Vth=',Vth

m=0.5d0+Atan(MINV)/pi

Vpoly=(q*epsi*NGATE*Coxe**2.d0*1.d6/2)*(Sqrt(1.d0+(2*Vgs-VFB-
PHIs)/(q*epsi*NGATE*Coxe**2.d0*1.d6))-1.d0)**2.d0
Vpolyeff=1.12d0-0.5d0*(1.12d0-Vpoly-0.001d0+Sqrt((1.12d0-Vpoly-
0.001d0)**2.d0+4.d0*0.001d0*1.12d0))

Vgse=Vgs-Vpolyeff

Voff1=VOFF+VOFFL/Leff

Vgsteff = (n*vt*log(1.d0+Exp(m*(Vgse-Vth)/n*vt)))/
(m+n*Coxe*Sqrt((2.d0*PHIs)/(q*NDEP*epsi))&
*Exp(-1.d0*((1.d0-m)*(Vgse-Vth)-Voff1)/(n*vt)))

!effective mobility
Ueff=U0/(1.d0+(UA+UC*Vbseff)*((Vgsteff+2.d0*Vth)/TOXE)+UB*((Vgsteff+2.d0*Vth)/TOX
E)**2.d0)

I0=Ueff*(W/L)*Sqrt((q*epsi*NDEP/(2.d0*PHIs))*vt**2.d0

!subthreshold leakage current
Ids(j,i)=I0*(1.d0-Exp(-1.d0*Vds/vt))*Exp((Vgs-Vth-Voff1)/(n*vt))

!write (10, *) Tcel, Ids
!print *, Tcel, Ids

End Do
End Do

print *, 'Vth=',Vth

Tcel=0.d0
Do i=1,140
Tcel=i+1.d0
write (10,*) Tcel, Ids(1,i), Ids(2,i), Ids(3,i), Ids(4,i), Ids(5,i)
End Do

End Program main

```