

Daniel Francisco GOMEZ-PRADO

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EDUCATIONAL BACKGROUND:

- **University of Massachusetts Amherst, MA (UMASS)**
 - PhD in Electrical and Computer Engineering exp May 2009
 - M.S. degree in Electrical and Computer Engineering GPA – 3.62 Feb 2006
- **San Marcos University, Peru (UNMSM)**
 - M.S. in Pure Mathematics. Dec 2002
 - B.S. degree in Electronic Engineering. Dec 2000

Relevant Courses: Intro to VLSI Design, Advanced VLSI Design, Computer Algorithms, Computer Architecture, Synthesis & Verification of Digital Designs, Reconfigurable Computing, Computer Networks, Advanced Computer Networks & Wireless Systems, Control Systems, Testing & Diagnosis of VLSI circuits, Entrepreneurial & Technological Management, Stock Analysis.

RESEARCH EXPERIENCE:

- **Research Assistant at University of Massachusetts Amherst** Jan 2004 ~ present
- **Implementation of the TEDify Software** Jan 2005 ~ present
Data path portion of behavioral design is extracted and represented in canonical Taylor Expansion Diagram (TED). The TEDify software reduces the number of operations in the data path by reordering its operations and performing common sub-expression elimination. It is applicable to ESL/behavioral synthesis, as different sequences of cuts in the TED graph define unique data flow graphs (DFGs). The software can be used to perform DFG optimization for delay, area and power. Other applications include: functional verification and code movement. The TEDify program can be found at:<http://tango.ecs.umass.edu/TED/Doc/html/index.html>
- **Mathematical Analysis of Taylor Expansion Diagrams (TED)** Feb 2004 ~ Dec 2005
The TED graph representation was studied and a mathematical model for variable ordering developed. The algorithm was implemented and integrated with the TEDify package. Part of this research was performed at LESTER Lab, Univ. of Bretagne Sud, France, June 2004, while studying the viability of TED as a data structure for encryption algorithms and Reed Solomon codes.
- **Soft-Cores vs. Hard-cores: a Synthesizable 8-bit Microcontroller** Sept ~ Dec 2004
Soft core FPGAs provide designers with flexibility of creating a perfect fit in terms of processor, peripherals and memory interfaces for their applications. This flexibility usually comes with a tradeoff in performance and cost. This research aimed at gaining some insights on these tradeoffs. A synthesizable microcontroller was developed.
- **Implementation of a Dynamic Scheduling Algorithm** Nov ~ Dec 2003
A Web-based implementation of the Tomasulo's algorithm for dynamic scheduling was developed as a tutorial for students of Computer Architecture.
- **Design of a Memory DRAM controller** Feb ~ Apr 2000
Embedded applications with Microcontrollers (μ C) usually suffer from limited memory. An interface

for the EDO DRAM memory with a μ C was designed and implemented in a CPLD from Cypress, coded at RTL level in VHDL. Research Assistant at the University EUTI, Spain.

PROFESSIONAL EXPERIENCE:

- **Intern at SYNPLICITY, USA** Jun 2006 ~ Sept 2006
A code in C was developed to traverse an RTL netlist provided to the Synplify Pro mapper tool, and detect whether or not an FIR filter exist inside the netlist. If an FIR exists, the instances that built it were marked and a new hierarchical view of the FIR component was created.
- **Digital Design Eng. at INICTEL, Peru** Jul 2000 ~ Jul 2001
Designing and implementing a text-based telephone for deaf people. Two microcontrollers, a master and a slave, were use to implement the terminals; DTMF encoders/decoders were used for Tx/Rx over the telephone network and keyboards and LCDs were used as input/output devices.
- **Instructor at San Marcos University, Peru** Jul 2001 ~ Jul 2004

PUBLICATIONS:

- Behavioral Transformations using Taylor Expansion Diagrams, DATE 2007.
- Optimum factorization of DSP transforms using Taylor Expansion Diagrams, DATE 2006.
- Embedded Systems and FPGA Soft-cores, UNMSM Magazine ISSN 1561-0853, 2006.
- Tutorial in FPGA routing, UNMSM Magazine ISSN 1561-0853, 2006.
- Variable ordering in Taylor Expansion Diagrams, HLDVT 2004.
- The VHDL language - Digital Design, book, 120 pages, 2003.
- VHDL Language Tutorial, UNMSM Magazine ISSN 1561-0853, 2003.
- The Pc Keyboard as data input to the PIC16F84A, UNMSM Magazine ISSN 1561-0853, 2002.
- Design of a text telephone for deaf, UNMSM Magazine ISSN 1561-0853, 2002.
- Design of a memory DRAM controller, UNMSM Magazine ISSN 1561-0853, 2001.

HONORS & AWARDS:

- Isenberg Scholar at UMASS for the Fall 2006 – Spring 2007 academic year.
- Graduate School Fellowship at UMASS, for the Fall 2006 – Spring 2007 academic year.
- Fulbright Fellow at University of Massachusetts, Amherst, Fall 2003 – Spring 2005.
- Concytec Fellow at San Marcos University (M.S. in Pure Mathematics), 2001 – 2002.
- ICTP grantee, the Seventh College, Real-time Microprocessor-based Systems on Physics, International Center for Theoretical Physics, Trieste – Italy, Oct – Nov 2002.
- AECI grantee to perform research in Spain, Feb – Apr 2000.

RELEVANT SKILLS:

Throughout the years I have work with different tools: Cadence tools for VLSI layout; HSPICE and IRSIM for CMOS analysis; Verilog and VHDL for behavioral and RTL descriptions; OrCad Layout for PCB routing; VPR for FPGA routing estimation; Synopsis DC, Altera Quartus, Xilinx ISE, Cypress Warp and Synplify for synthesis; Assembly languages (Microchip, Intel x86) for RISC and CISC μ C programming; Lex and Yacc for parsing; Matlab for modeling. Additional skills include:

- C/C++, STL library, garbage collection, OOP, cross-platform app, svn. (biggest code 15k lines)
- Java, stand alone and Applet applications with some knowledge of Java Servlets and Movil.

REFERENCES:

- Prof. Maciej Ciesielski, telephone: (413) 545-0401, email: ciesiel@ecs.umass.edu
- Prof. Wayne Burleson, telephone: (413) 545-2382, email: burleson@ecs.umass.edu