Full Copper Wiring in a Sub-0.25 μm CMOS ULSI Technology

D. Edelstein*, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt†, W. Motsiff†, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz , L. Su, S. Luce†, and J. Slattery†

IBM Semiconductor Research and Development Center, Hopewell Junction, NY 12533
†IBM Microelectronics, Essex Junction, VT 05452
**Phone: (914) 945-3051: FAX: (914) 945-4015: E-mail: edelstn@watson.ibm.com*

Abstract

We present the first fully integrated ULSI CMOS/ copper interconnect technology. Up to 6 Cu wiring levels are built at minimum metal-contacted pitch of 0.63 μm, with W local-interconnect and contact levels and a poly-contacted pitch of 0.81 μm, on a fully-scaled sub 0.25 μm, 1.8V CMOS technology. The Cu wiring has advantages of significantly lower resistance, higher allowed current density, and increased scalability, relative to comparable Ti/Al(Cu) wiring[1]. These benefits in turn have enabled the scaling of pitch and thickness, from reduced-capacitance, high-density lower levels to low-RC global wiring levels, consistent with high-performance and high-density needs. The integrated Cu hardware was evaluated according to a comprehensive set of yield, reliability, and stress tests. This included fully functional, high-density 288K SRAM chips which were packaged into product modules and successfully tested for reliability. Overall, we find the results for full Cu wiring meet or exceed the standards set by our Al(Cu)/W-stud technology.

Device Technology

The key parameters of this technology are summarized in Table I[2,3] along with comparable values for the 0.25 μm technology that is currently in production. Figure 1 shows an SEM section of a device contacted at minimum pitch. Figures 2 and 3 show device current-drive and subthreshold performance for NFET and PFET devices built with this technology. Aggressive vertical and lateral dopant engineering leads to excellent short-channel effects and current-drive characteristics, even down to below 0.10 μm effective channel length[2]. The aggressive pitches and use of W damascene local interconnects allow for a 6-transistor SRAM cell size of only 6.8 μm^2, as described in ref. 4. As indicated in Table I, metal pitches range from 0.63 to 0.81 μm for up to 6 levels, with optional 2x-scaled pitch/thickness at M5 and M6 for very-low RC applications.

Cu Interconnect Technology

The Cu dual-damascene process[5] (inlaid, planarized metal in via/line insulator cavity) is employed for the 6-level builds shown in fig. 4 (all thin wires), fig. 5 (2x-scaled low-RC 5th and 6th levels), and fig. 6 (1x- and 2x-scaled via-chains). This is accomplished by chem-mech polishing of an electrolytically-plated Cu fill. The electro-plated Cu process has exceptional pattern-filling capability, as indicated by fig. 7. This TEM section shows an 0.2 μm reentrant profile in polyimide, filled in a void-free manner with plated Cu. The plated Cu consistently shows a 1.8 μΩ-cm resistivity, and the composite interconnects (with liner) range from 1.9 to 2.2 μΩ-cm for thicker or minimum lines, respectively; this is a 40-45% drop from comparable Ti/Al(Cu)/Ti lines. Figure 8 shows Cu vs. Al(Cu) 0.63 μm pitch M1 wire resistances; here the Cu was scaled such that R is reduced by 25% and C by 15%. The Cu via contact resistances are about half that of the Al(Cu)/W-studs, as shown in fig. 9 for long via-chains from several wafer lots. Figure 10 shows wafer lot yields for large M3 mazes at minimum pitch, built on all the lower wiring levels. The good yields indicate a robustness of the integration process against intra- and interlevel defects.

Reliability

The integrity of the CMOS/Cu integration was evaluated using key reliability and stress tests on a variety of structures, circuits, and packaged modules. In many cases, control samples with Al(Cu)/W wiring on identical chips were included. Table II shows product functional stress results on 288K SRAM chips with all Cu wiring (from two populations of hardware) that were packaged into wirebond modules. The SRAMs were of the minimum 6.8 μm^2 cell design, embedded within and diced out of larger test chips. All SRAM chips were fully functional after passing high voltage screening (except as noted) prior to the stresses shown. The voltage-screened Cu parts showed only one fail after extended functional stress at 2.7V/140°C operation and no fails after 200 thermal cycles. These results showed statistically equivalent reliability to the Al(Cu) hardware that was run in parallel. This, we believe, is the first report of a CMOS/ Cu-wiring technology carried through product-like chip, package, and burn-in conditions.

Test-chips and SRAMs with Cu last-metal levels were also assembled into C4 "flip-chip" modules, and passed thermal cycling (T/C), "highly-accelerated stress-test" (HAST), temperature/humidity/bias (T/H/B), and SRAM

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functional tests. In all of the module types tested, the Cu/C4 modules had equivalent reliability (N_{50}, σ) to the Al(Cu)/C4 controls, where the C4 fatigue life is the limiting factor. Fig. 11 shows one of the C4 solder balls on Cu wiring after 10 reflow cycles to 375°C, to test for fails by Cu(Sn) intermetallic formation in the wiring; no such fails have been found in any of the stressed hardware.

The potential for Cu contamination of the MOS devices was investigated aggressively, for example with high temp/bias stresses on devices with large-area exposure to the Cu wires. Fig. 12 shows leakage data from 236K μm^2 p^+-poly/gate-ox/diffusion capacitors after stress, showing no Cu vs. Al(Cu) anomalies. Large numbers of several device types were stressed for 300 hrs. at 140-290°C, with M1 biases from -2 to -50V (to drive any Cu^+ ions towards the gates or junctions). Devices included large-area, plate or fingered diffusion capacitors, NFETS, and PFETS under large-area Cu M1 plates or fingers. Some structures had intentional line/stud misalignment, in an attempt to promote defects. Figure 13 shows an example of Cu plate/NFET junction leakage vs. time at 30V/250°C stress, showing no shifts. In all, 720 chips from several wafer lots were tested, and no fails by Cu poisoning were found.

The Cu wiring itself was also stress-tested extensively. Intrinsic Cu reliability, such as electromigration resistance, was confirmed to be orders of magnitude better than for Ti/Al(Cu)/Ti, as reported previously[5]. Figure 14 shows electromigration data for the worst-case situation tested here: 0.3 μm single-damascene M1 lines on W-studs, at 295°C, and with 2.5MA/cm^2 stress current. The T_{50} lifetime is >100x longer for Cu than for our best Ti/Al(Cu)/Ti lines. The Cu lifetime improvement is even greater for the other line levels, and at lower temperatures (higher Cu activation energy), and projects to several orders of magnitude longer lifetimes for Cu at chip-use conditions. This supports a much higher current density spec and underpins the extendability of our Cu wiring for future pitches, higher performance, and scaling of line cross-sections to minimize capacitance and crosstalk. Also, high-current needs for the upper wiring levels, such as DC power distribution, off-chip I/O, etc. can be done at greatly increased wiring density relative to Al(Cu).

Another intrinsic wiring reliability issue is stress-migration, or the slow formation of voids in fine lines under tensile stress at chip operating temperatures. Figure 15 shows resistance vs. square root of time (to show any straight-line diffusive response) for 20 chips each of Cu vs. Al(Cu) in specialized test structures. These structures simulate high-fanout from a single contact stud with 0.3 μm lines, and respond more strongly than typical chip wiring to stress-voiding. Parts were stored at 225°C (predicted maximum stress-migration temp) for thousands of hours, with periodic readouts. The upper traces show large resistance rises and scatter for Al(Cu) lines in this structure; this typical response has been correlated with stress-voiding. In sharp contrast, there is no rise or scatter at all in the Cu lines, even after 5000 hrs.; the Cu resistance actually decreases slightly, due to annealing. Post-analysis confirmed no stress-voiding in the Cu lines. This Cu benefit is especially important for the future, as stress-voiding is projected to be more severe for decreasing linewidths in Al(Cu)[6].

"Extrinsic" reliability that relates to the integration, such as corrosion, defects, or weak interfaces, was evaluated by extended T/H/B and T/C stresses on 3- and 6-level Cu hardware. For example, T/H/B stress was done on 100 modules for 1000 hrs. at 85°C/85% r.h./3.6V, with no fails found in any of the devices tested. An example of T/C stress results is shown in table III, where 11,400 Cu multilevel line/stud structures were subjected to 1,550 shallow and deep thermal cycles, with no fails. The T/H/B results also found no fails for Al(Cu) or Cu hardware after 1000 hrs. at 85°C/81% r.h./3.6V. These defect-sensitive, no-fail results meet (at least) the expectations for the Al(Cu)/W wiring, and indicate a lack of significant weaknesses in the Cu integration scheme.

In summary, a full copper/CMOS integrated circuit technology is presented. The key integration and reliability issues are addressed, with results that demonstrate the feasibility of copper interconnects for CMOS ULSI applications.

Acknowledgements

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Parameter	This paper	Current Production
Supply voltage	1.8V	1.8V
I/O voltage (max)	3.3V	3.3V
Gate length (drawn)	0.20 μm	0.25 μm
Channel length (effective)	<0.15 μm	0.15 μm
Gate ox. thickness	35 Å	40 Å
# Metal layers	6	6
M1 contacted pitch	0.63 μm	0.7 μm
M2-M6 cont. pitch*	0.81 μm	0.90 μm
Metal	Cu	Al(Cu)
Local Interconnect?	Yes	Yes
SRAM cell size	6.8 μm^2	8.6 μm^2

**optional 2x-scaled thickness/pitch M5, M6 for low-RC*

Table I. CMOS Technology parameters.

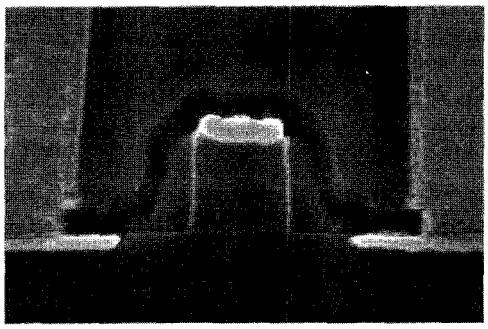

Figure 1. SEM of 0.20 μm MOSFET with minimum-pitch contacts.

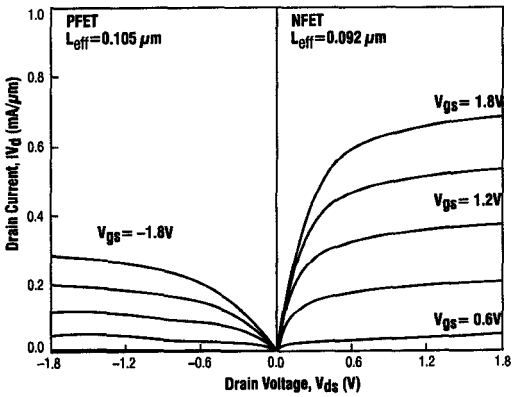

Figure 2. I_d-V_{ds} characteristics of NFET and PFET devices ($|V_{gs}|$=0-1.8V, 0.3V steps).

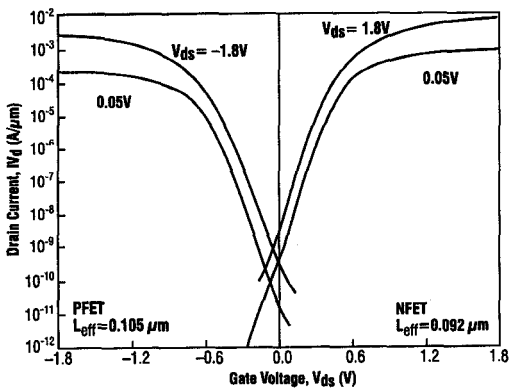

Figure 3. Subthreshold characteristics of NFET and PFET devices.

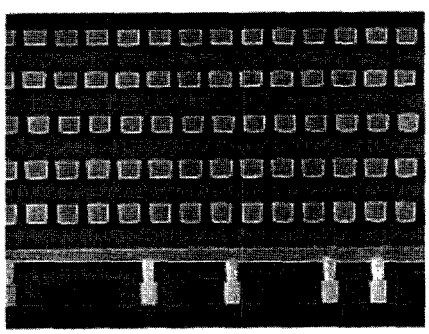

Figure 4. SEM of 6-level thin-wire Cu build. M1 Cu (transverse) is connected by W-studs to W local-interconnects.

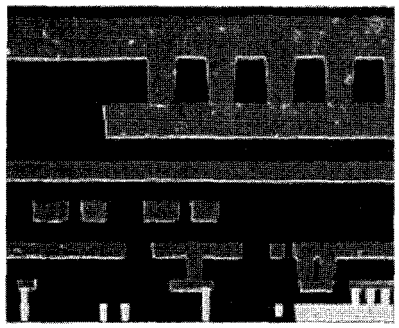

Figure 5. SEM of 6-level Cu build with 2x-scaled, low-RC M5 and M6.

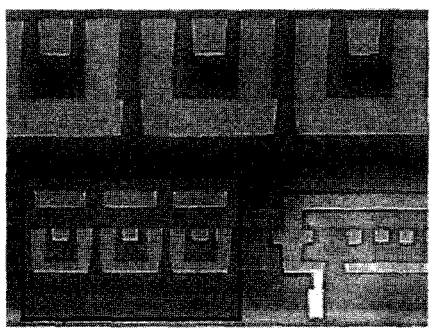

Figure 6. SEM views (same magnification) of 1x- (inset) and 2x-scaled dual-damascene intertwined via-chains.

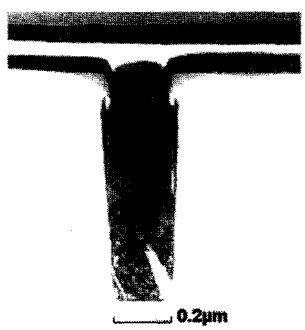

Figure 7. TEM of electroplated Cu fill in 0.2μm, 4:1 reentrant polyimide test via.

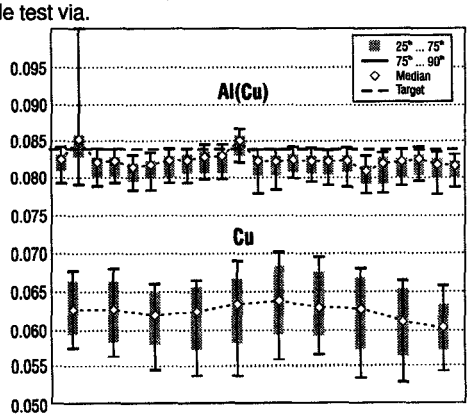

Figure 8. Sheet-resistance data by wafer for M1 Cu vs. Al(Cu) 0.32μm lines.

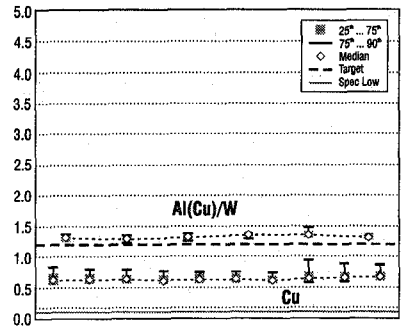

Figure 9. Resistance/link for Cu vs Al(Cu)/W via chains.

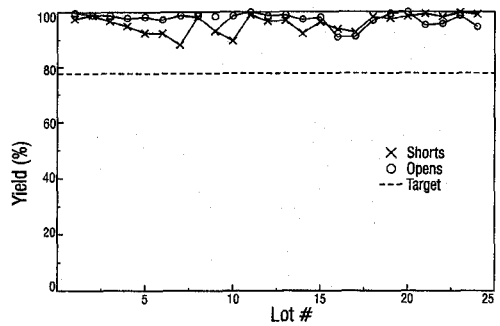

Figure 10. Wafer lot yield trend for large-area, minimum-pitch M3 mazes in multilevel Cu builds.

Stress	Group 1 Fails	Group 2 Fails
2.3V/100°C/5 hrs	0/149	1†,1†/247
2.7V/014°C/5 hrs	0	1,1†
2.7V/014°C/144 hrs	0	0
2.7V/014°C/5000 hrs	0	–
0-125°C Thermal Cycle 20X	0	0
-40–150°C T/C 20X	0	0
-40–150°C T/C 200X	0	–

†This chip was not voltage-screened

Table II. Functional stress results on 288K SRAM modules with Cu wiring.

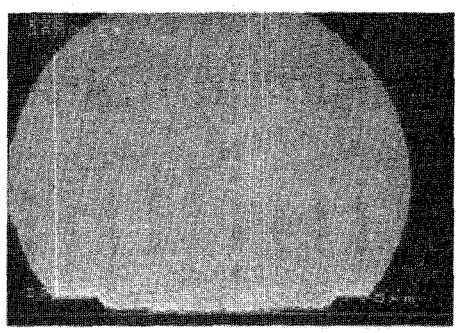

Figure 11. SEM section of C4 Pb(Sn) solder-ball on Cu wiring after 10 reflow cycles to 375°C.

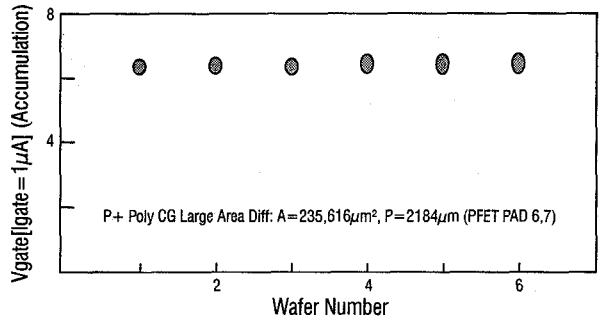

Figure 12. Large-area p+-poly/gate oxide/ diffusion capacitor leakages after voltage-ramp stressing for wafers with Al(Cu) (#1-3) or Cu (#4-6) 3-level wiring.

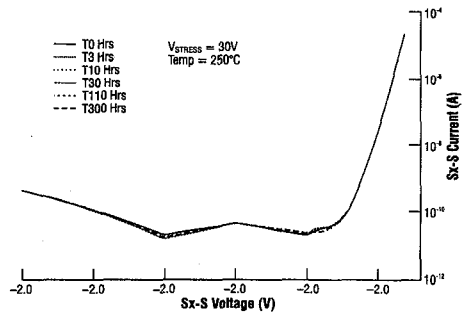

Figure 13. NFET/Cu device substrate-source (Sx-S) junction leakage after time intervals shown at 250°C/30V stress.

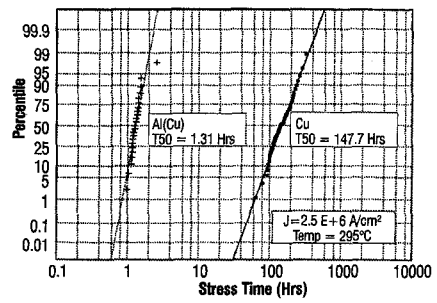

Figure 14. Electromigration data at 295°C, 2.5 MA/cm² for Cu vs. Al(Cu) 0.3 μm multilevel lines.

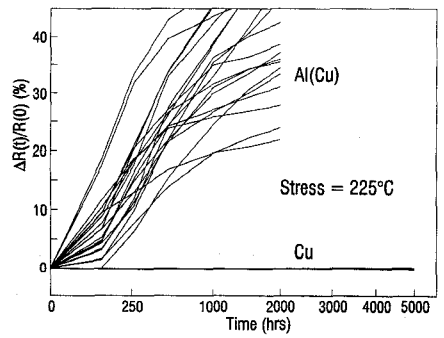

Figure 15. Stress-migration test structure resistance vs. square-root time for Cu vs. Al(Cu) 0.3 μm lines (20 chips each).

Stress	# Cu Fails
-65–150°C T/C 1000X	0/11,400
-165–180°C T/C 350X	0
-160–300°C T/C 200X	0

Table III. Thermal-cycle stress results on 3- and 6-level Cu via chains.